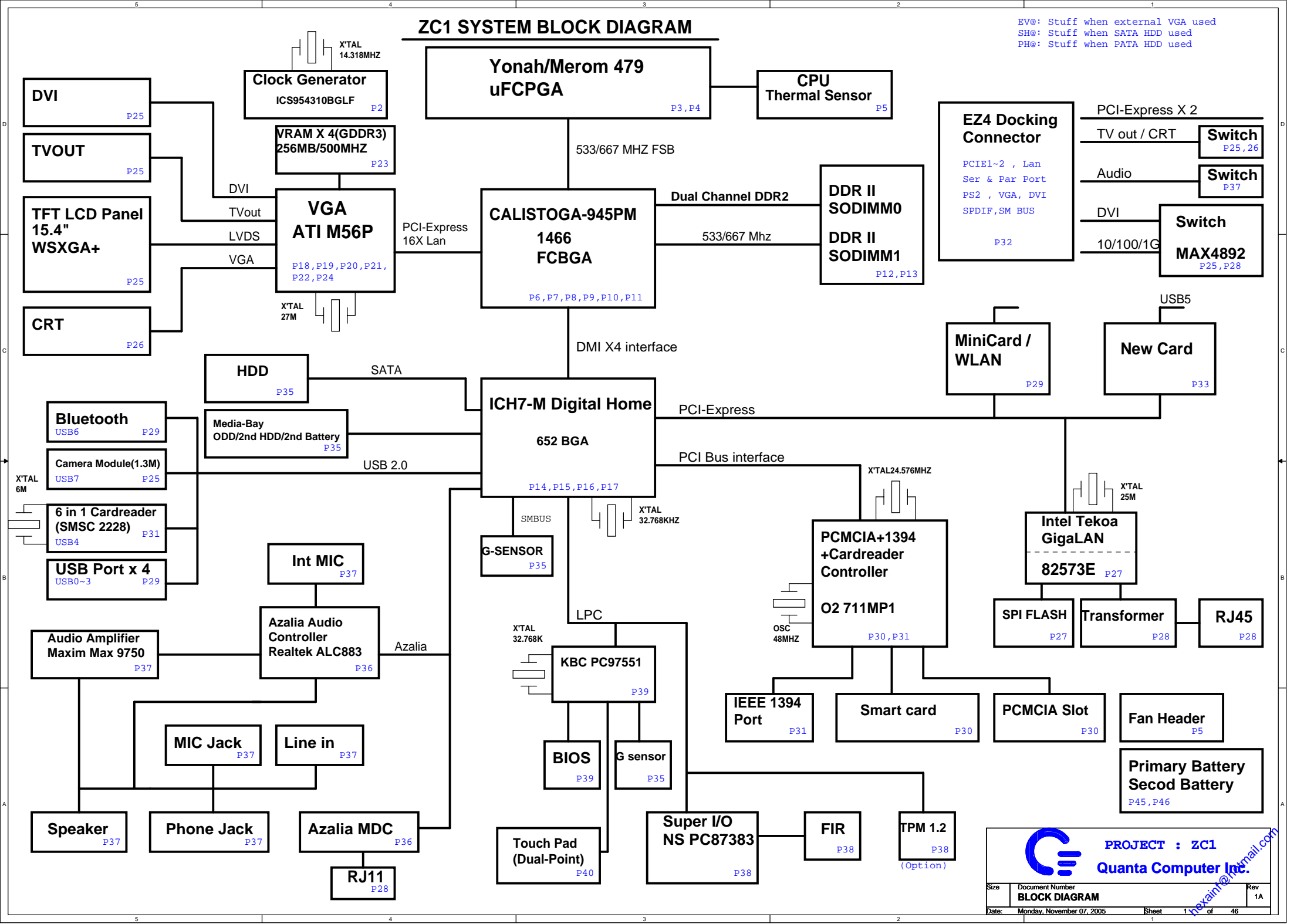


# ZC1 SYSTEM BLOCK DIAGRAM

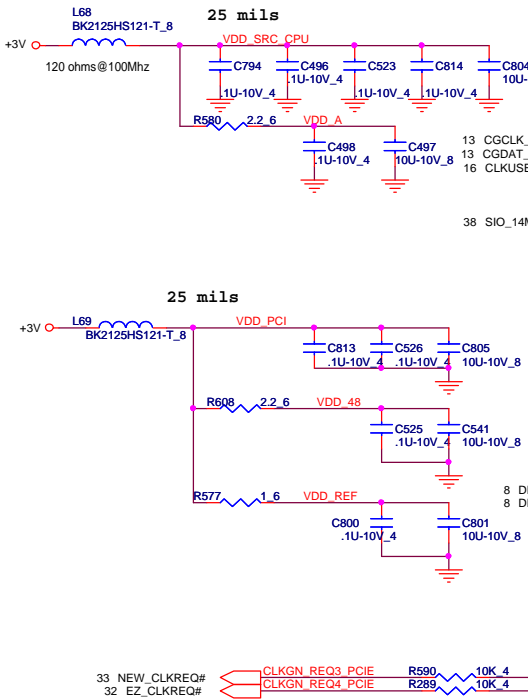
EV@: Stuff when external VGA used  
SH@: Stuff when SATA HDD used  
PH@: Stuff when PATA HDD used



PROJECT : ZC1  
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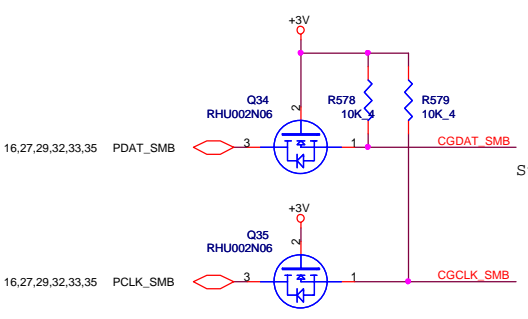
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	200	100	33

Default

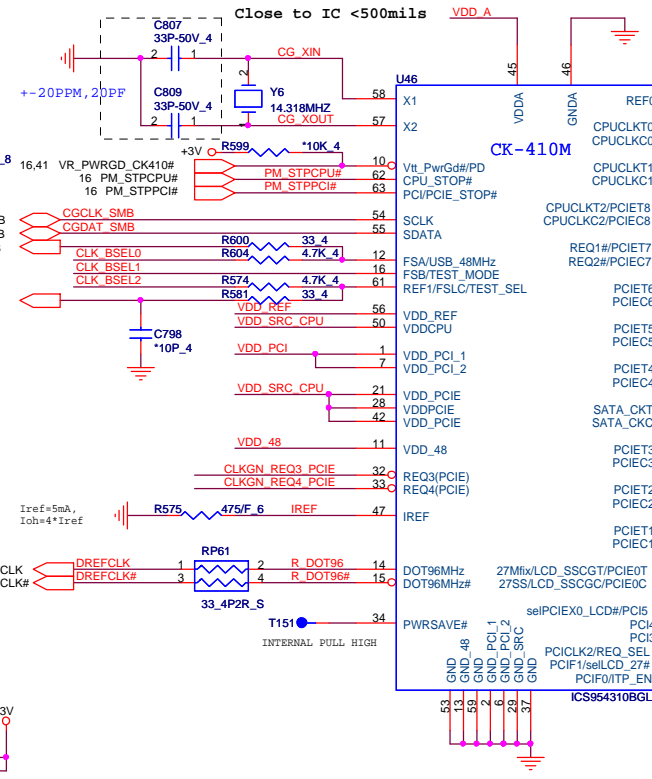


PREQ3(PCIE) Latched Select  
"0" : CLK Enable  
"1" : CLK Disable Control : PCIE 2,4,6,8

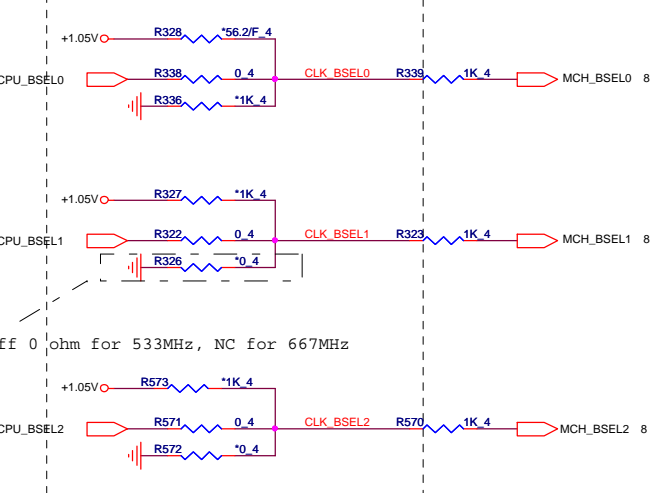
PREQ4(PCIE) Latched Select  
"0" : CLK Enable  
"1" : CLK Disable Control : PCIE 1,3,5,7



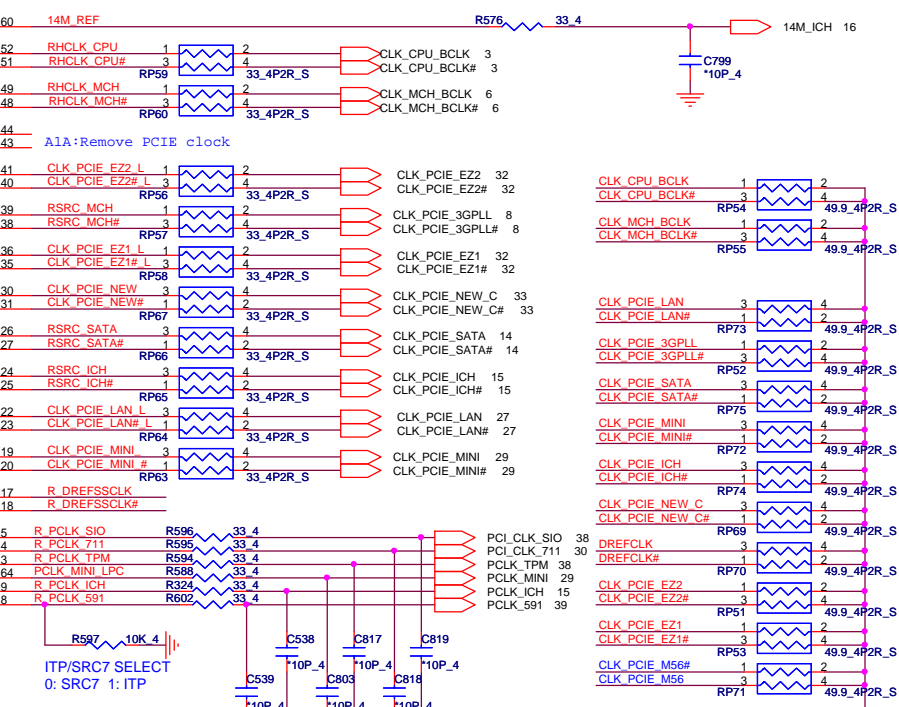
AlA-change X1,X2 capacitor from 27pf to 33pf(CL=20pf)



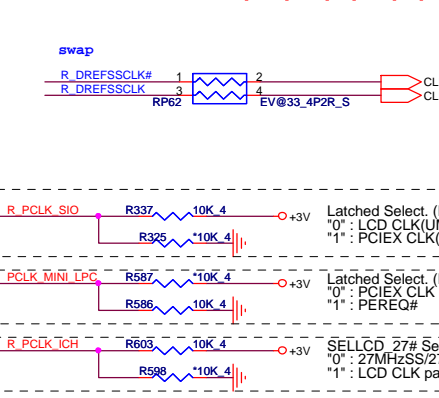
AlA-FSB Frequency Select:by CPU driven




Place these termination to close CK410M.



AlA:Change pin 3 PCLK\_LAN to PCLK\_TPM

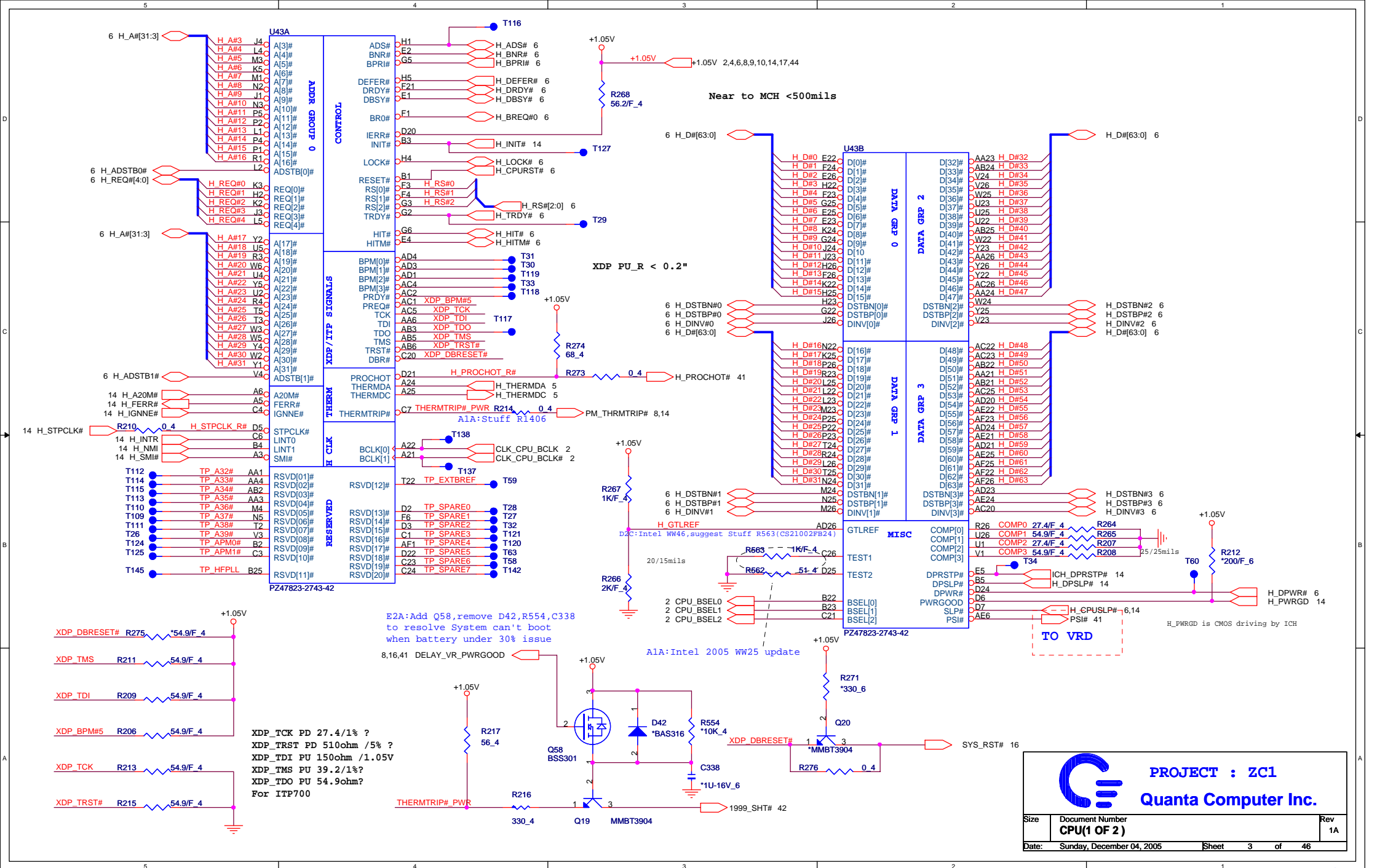




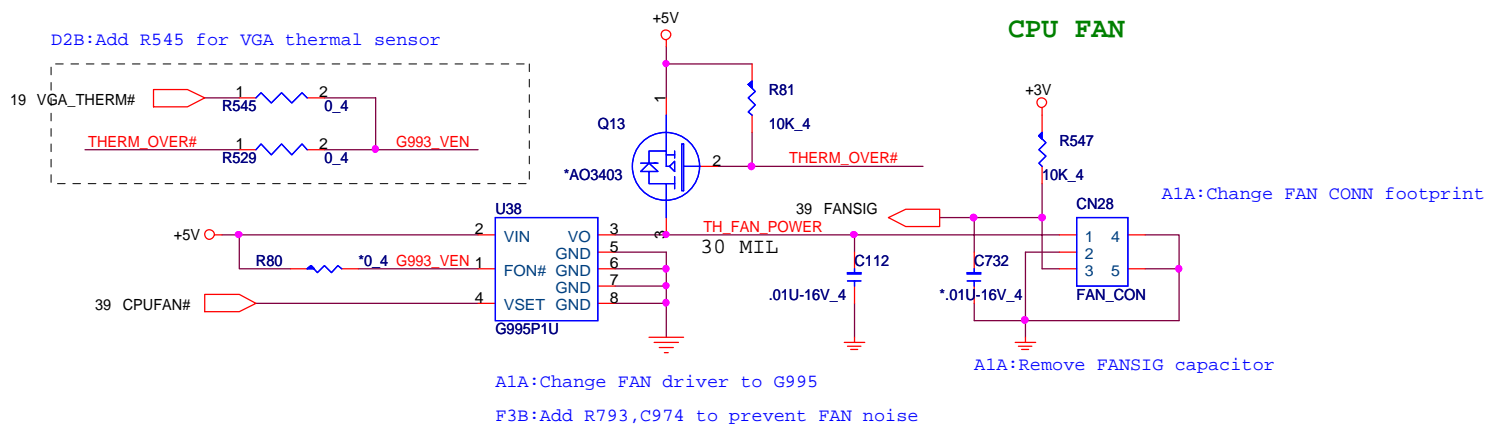
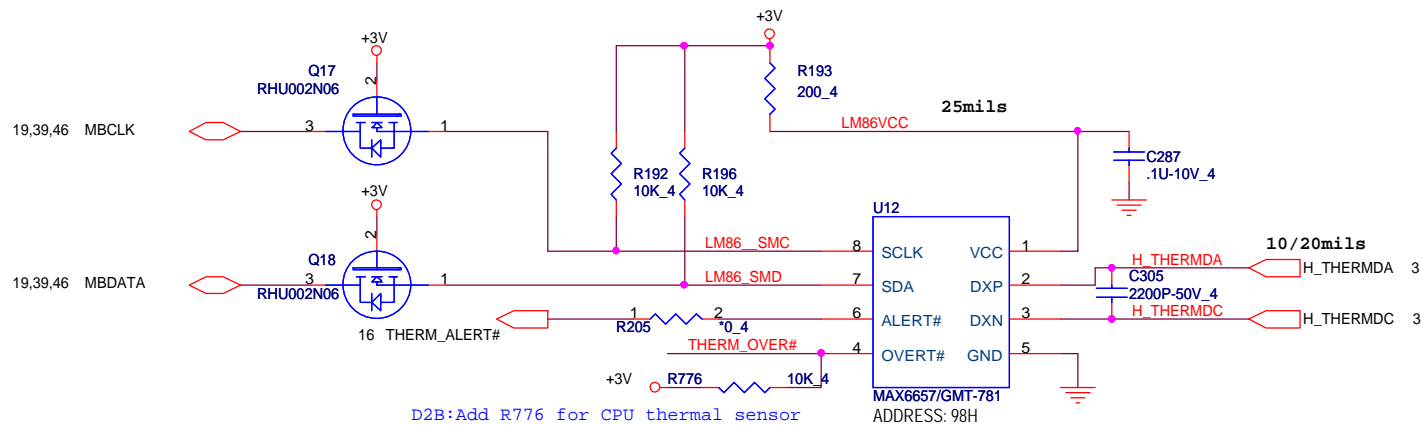
PROJECT : ZC1


Quanta Computer Inc.

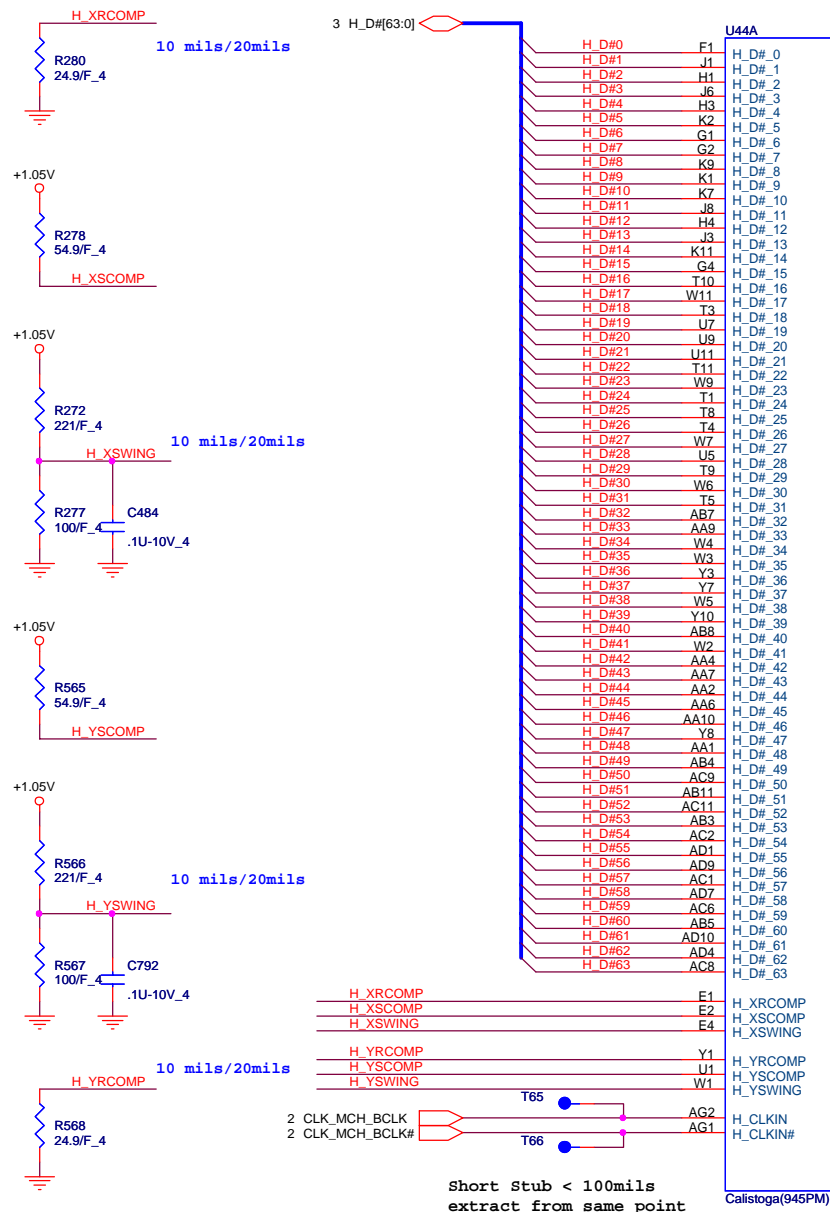
Size	Document Number	Rev
	CLOCK GENERATOR	1A
Date:	Friday, December 09, 2005	Sheet 2 of 46



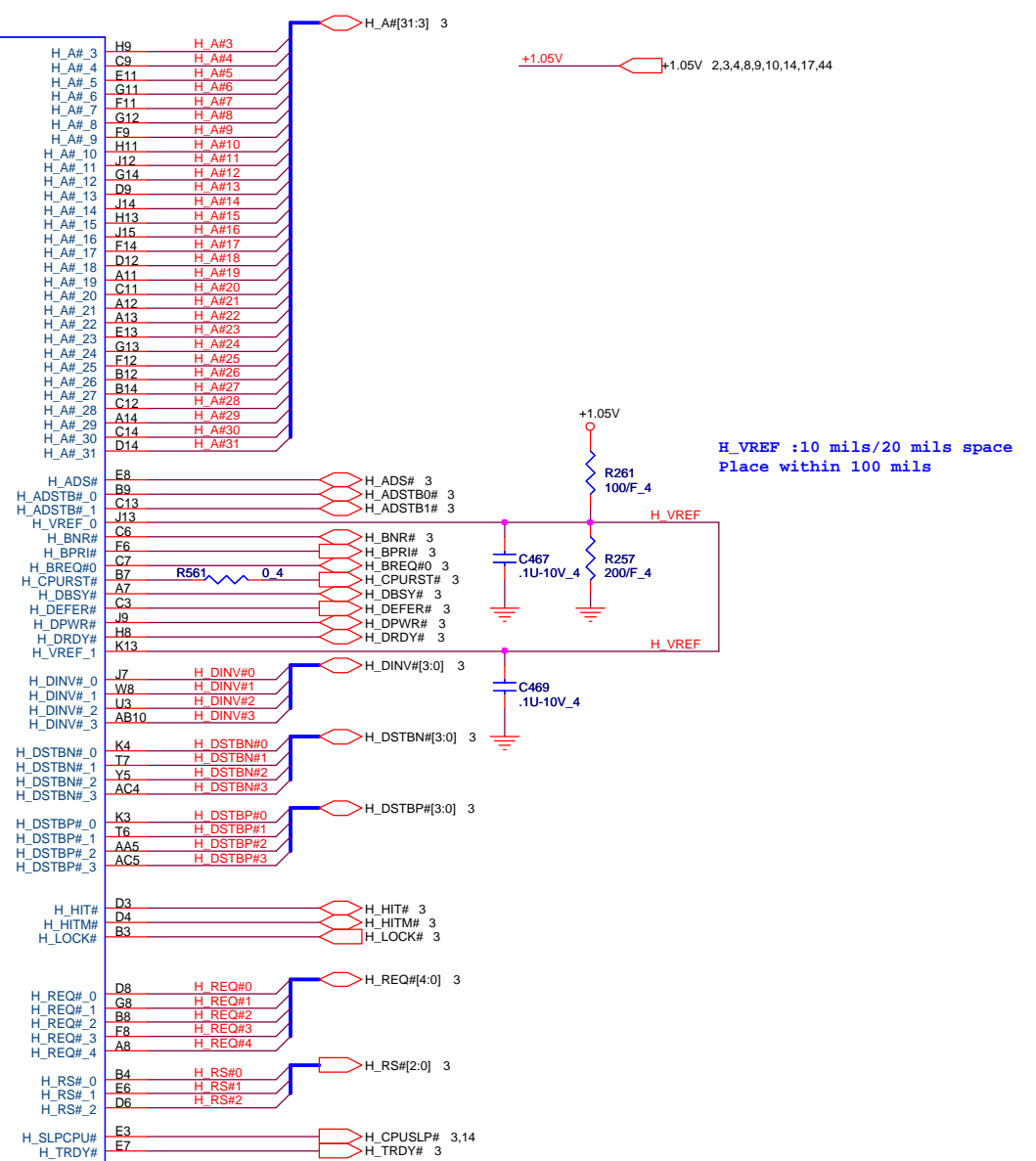




 <b>PROJECT : ZC1</b> <b>Quanta Computer Inc.</b>		
Size	Document Number	Rev
	<b>Thermal Sensor,FAN</b>	<b>1A</b>
Date:	Friday, December 02, 2005	Sheet 5 of 46

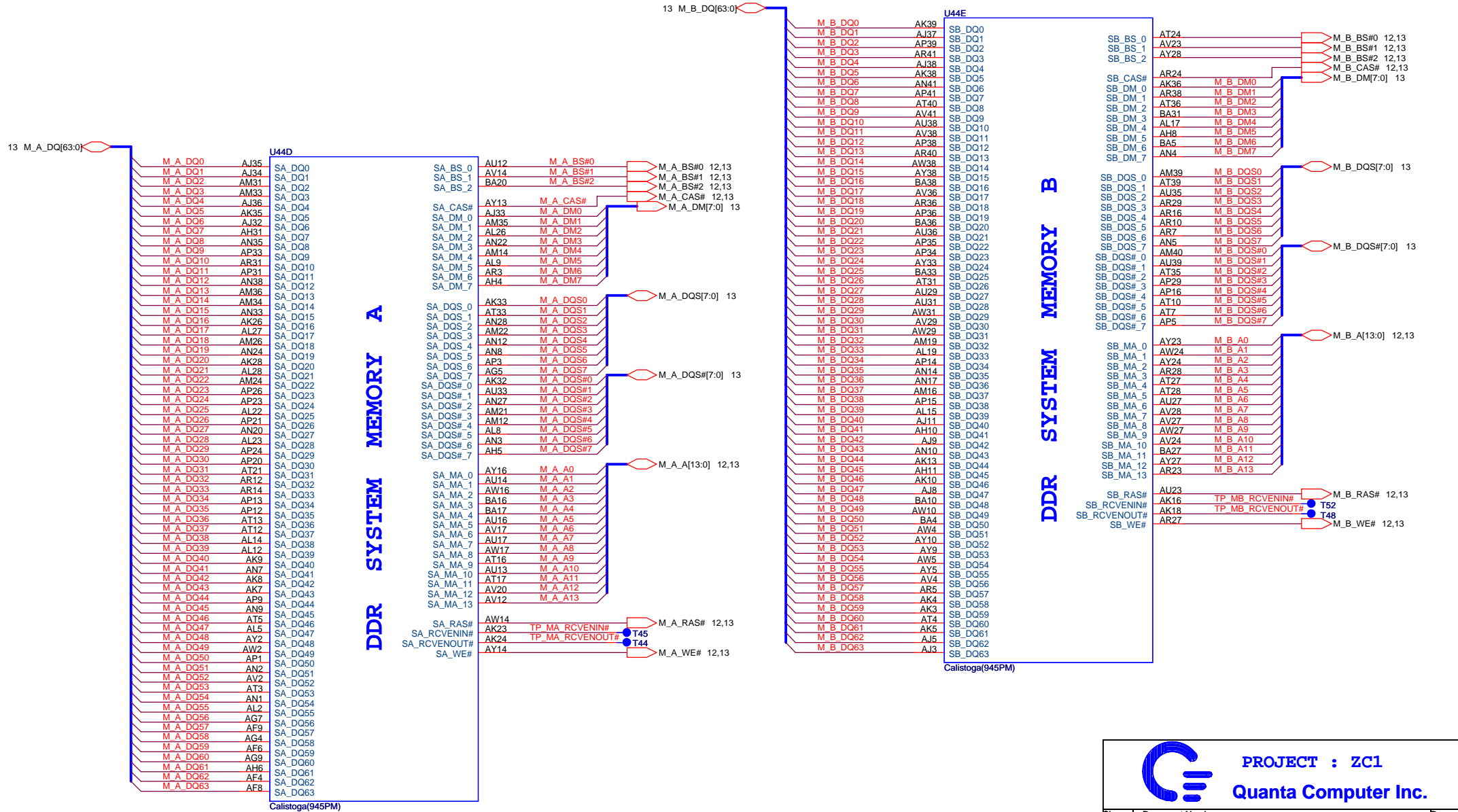


HOST

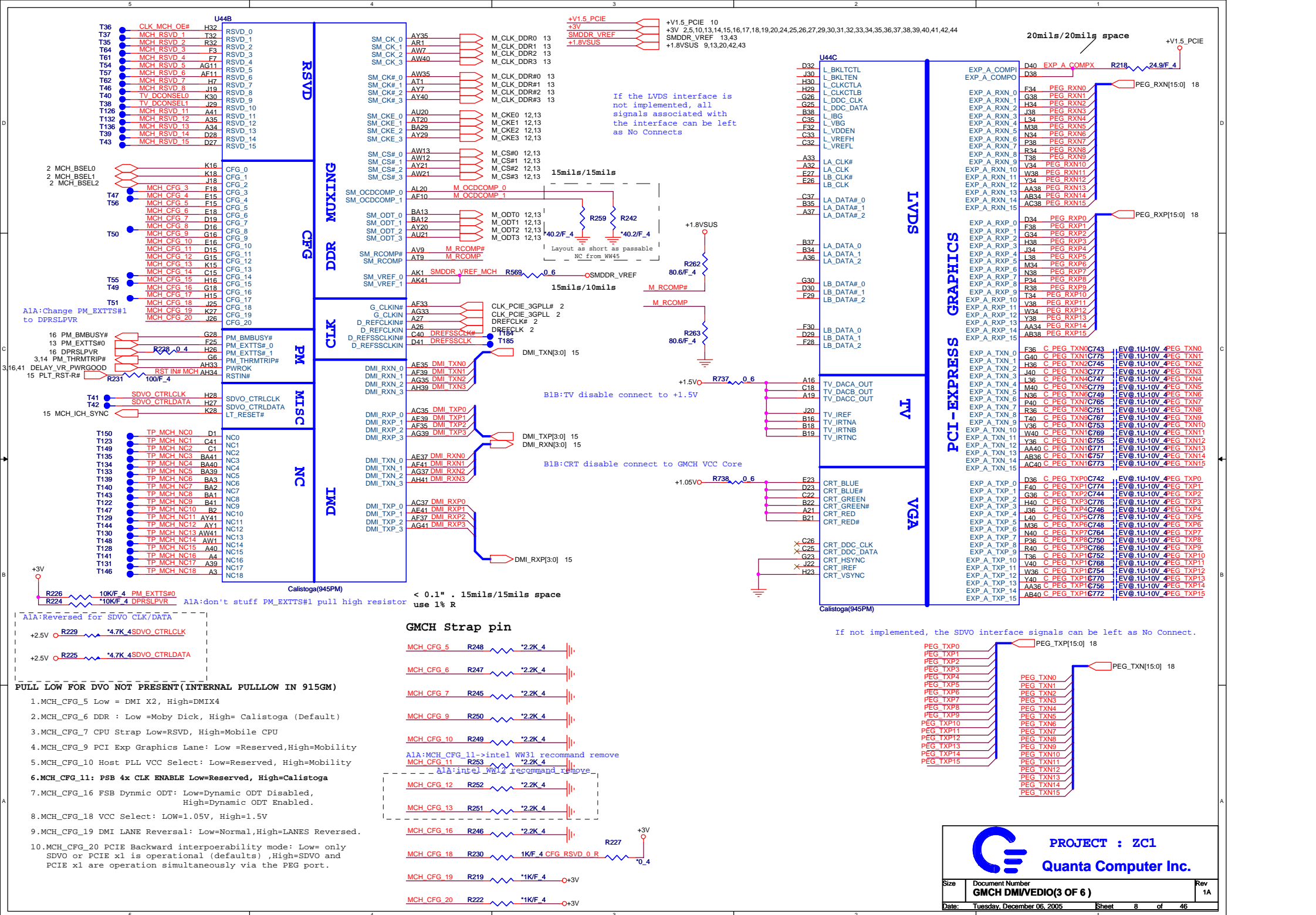


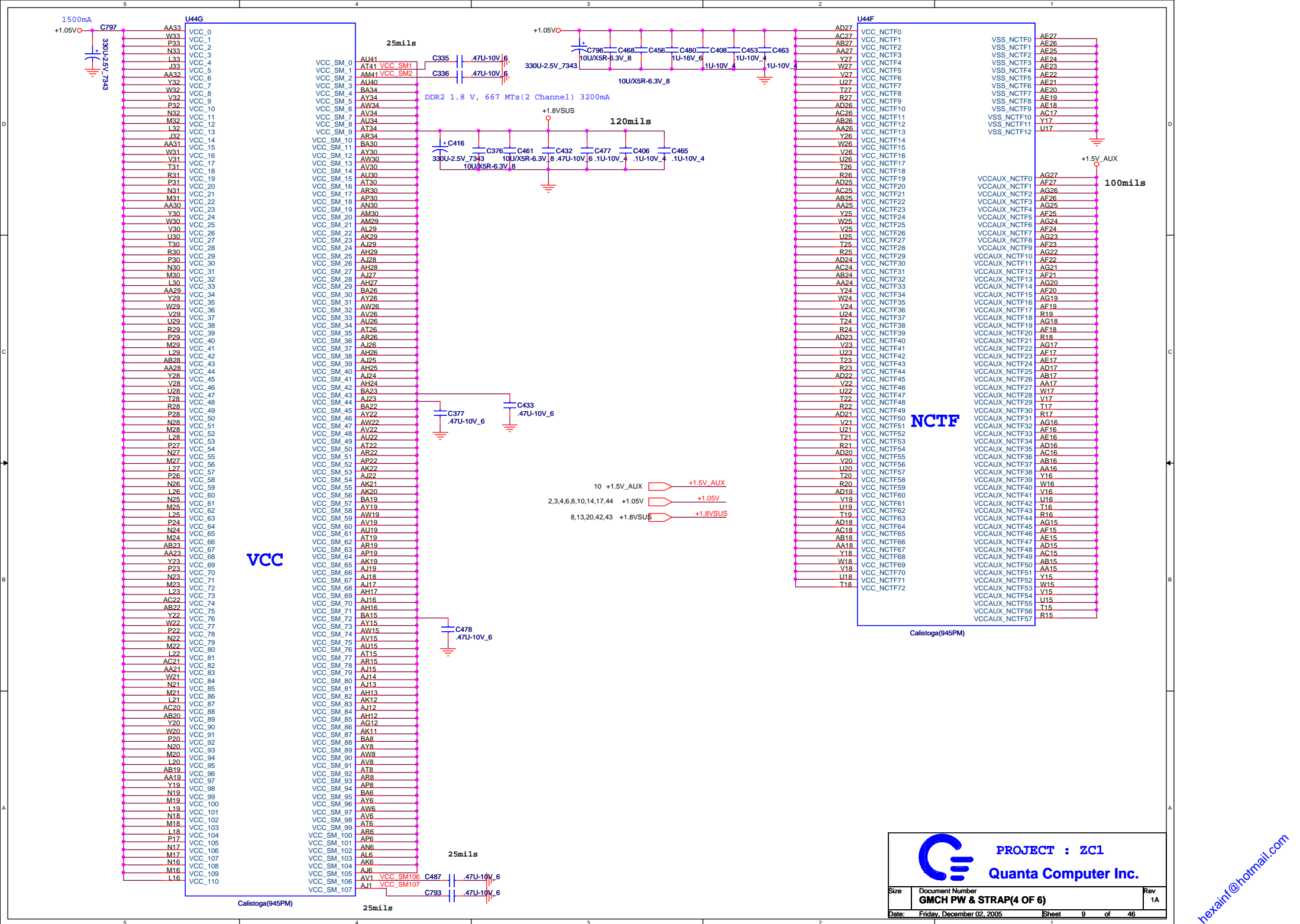
PROJECT : ZC1  
Quanta Computer Inc.

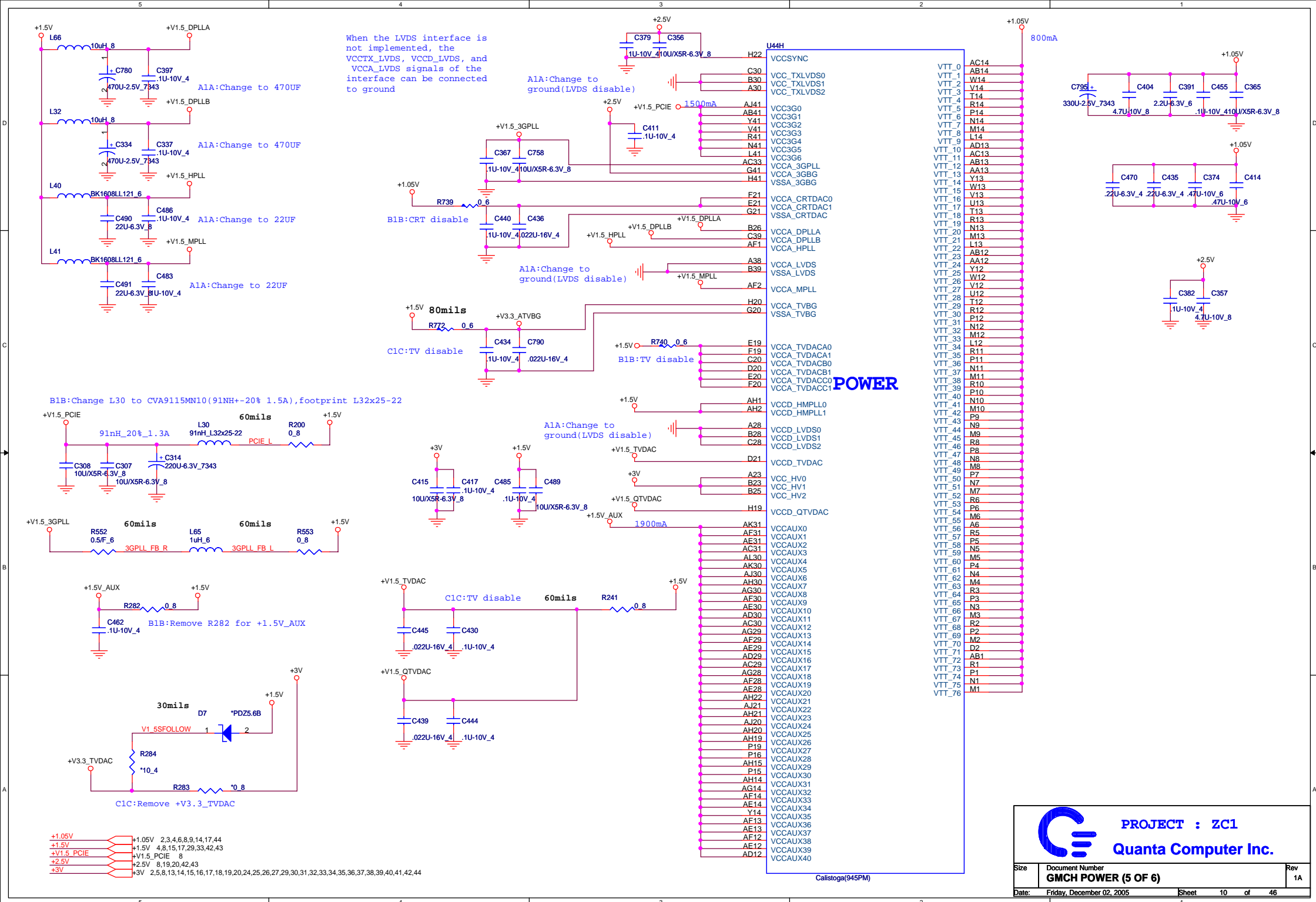
Size	Document Number	Rev
	GMCH HOST(1 OF 6)	1A
Date:	Friday, December 02, 2005	Sheet 6 of 46

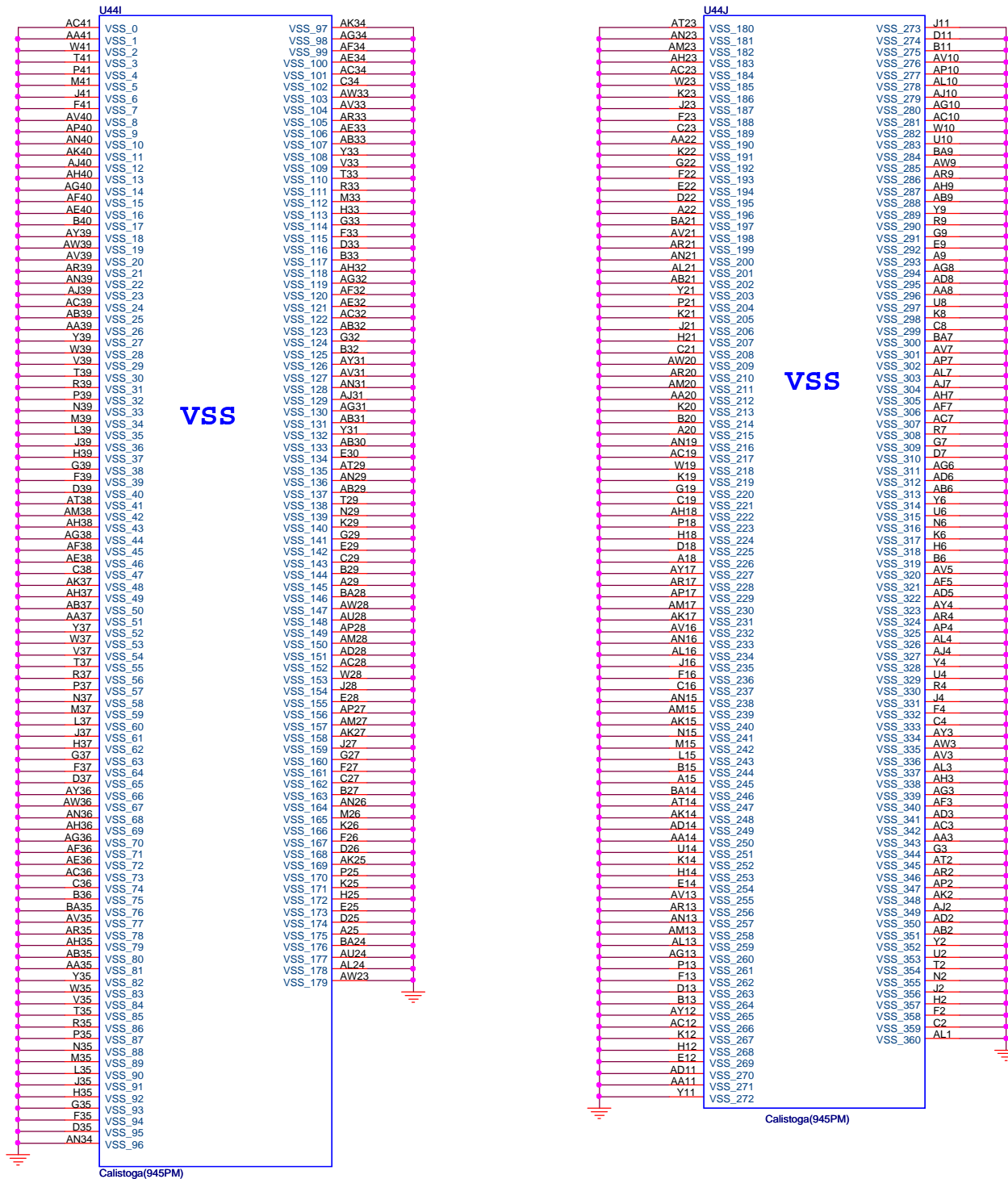


hexainf@hotmail.com



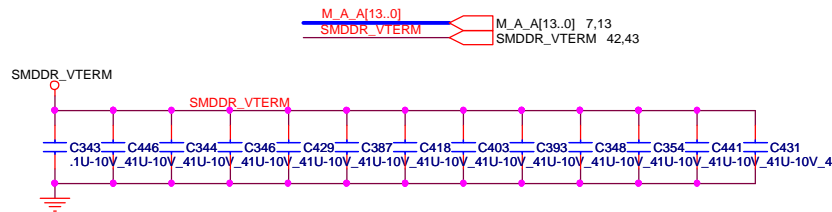




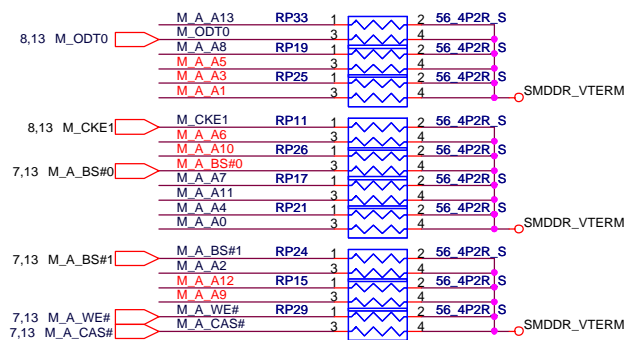


# DDRII DUAL CHANNEL A,B.

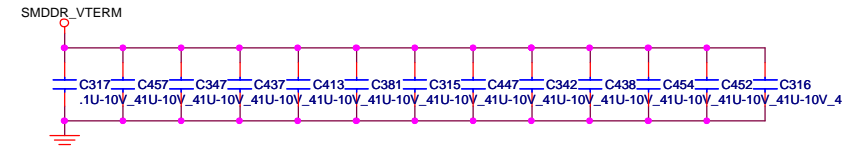
## DDRII A CHANNEL



A1A:Swap net

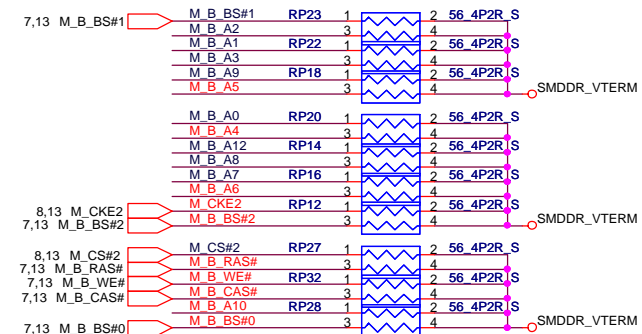


## DDRII B CHANNEL

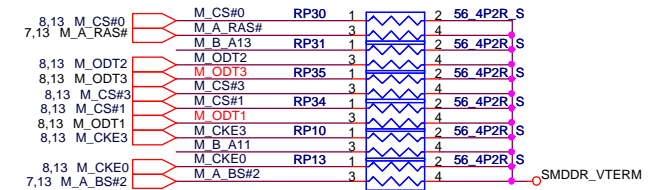


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR\_VTERM

A1A:Swap net

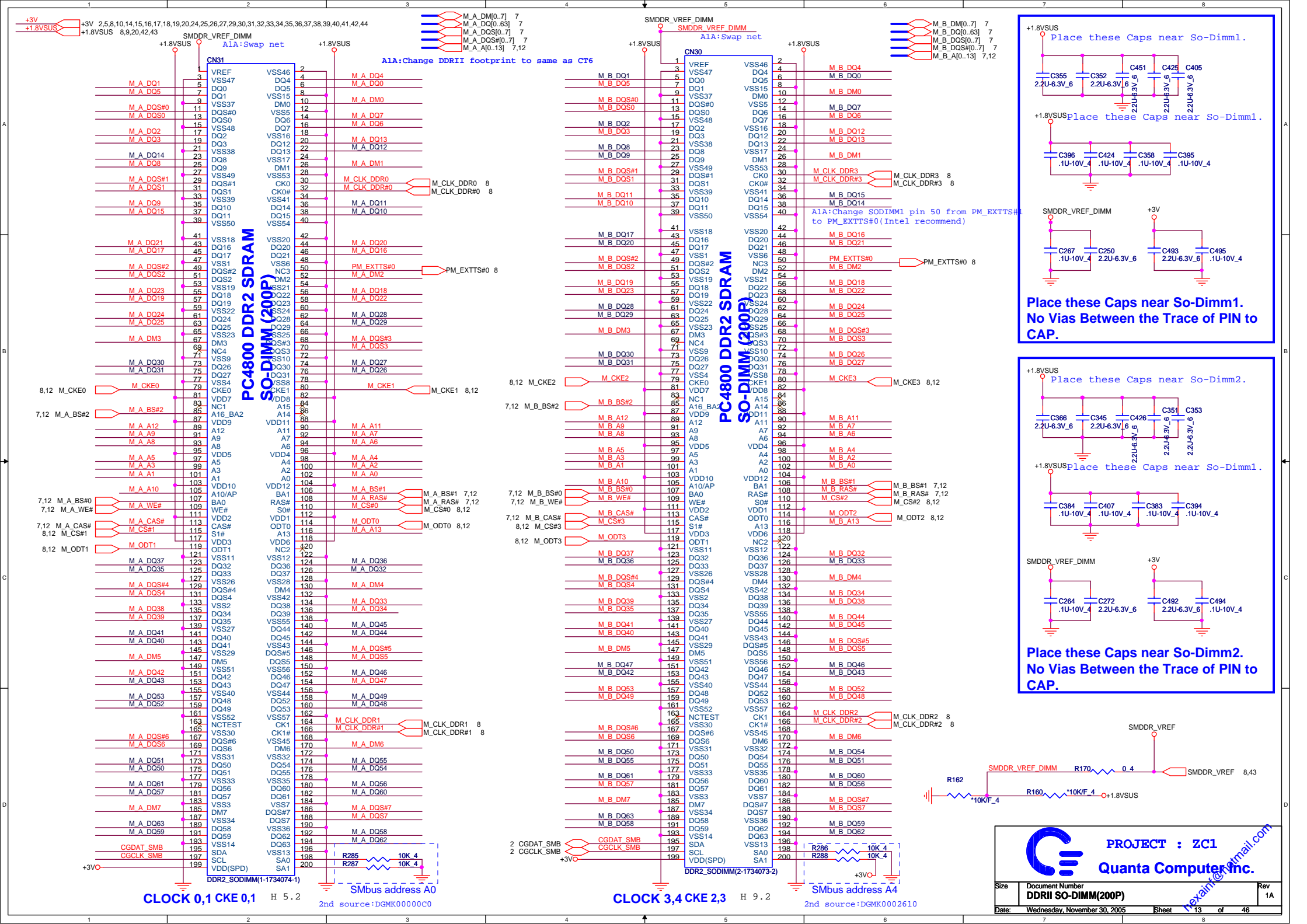


A1A:Swap net

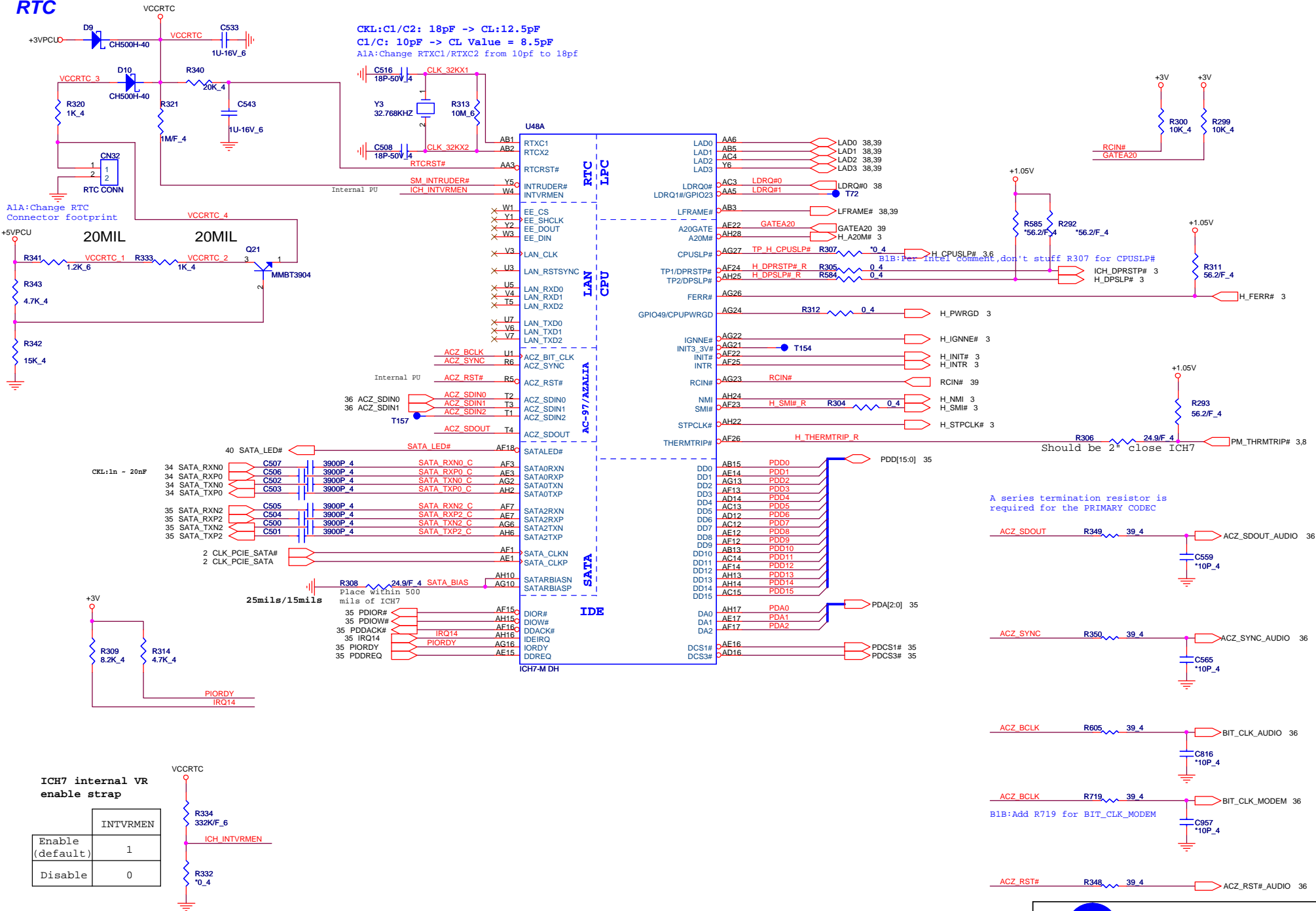


PROJECT : ZC1  
Quanta Computer Inc.

Size	Document Number	Rev
	DDR RES. ARRAY	1A
Date:	Monday, November 28, 2005	Sheet 12 of 46



**RTC**



PROJECT : ZC1  
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Size	Document Number <b>ICH7-M HOST (1 OF 4)</b>	Rev 1A
Date:	Friday, December 02, 2005	Sheet 14 of 46

ALA:Change PCIE pin define to meet Acer spec

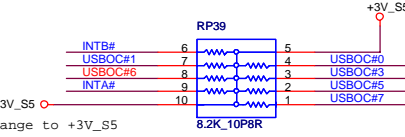
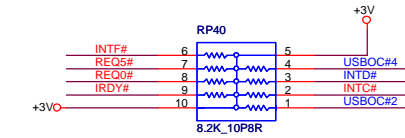
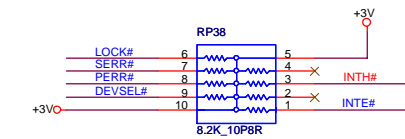
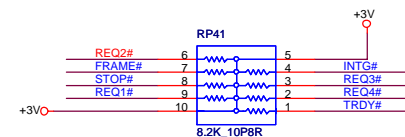
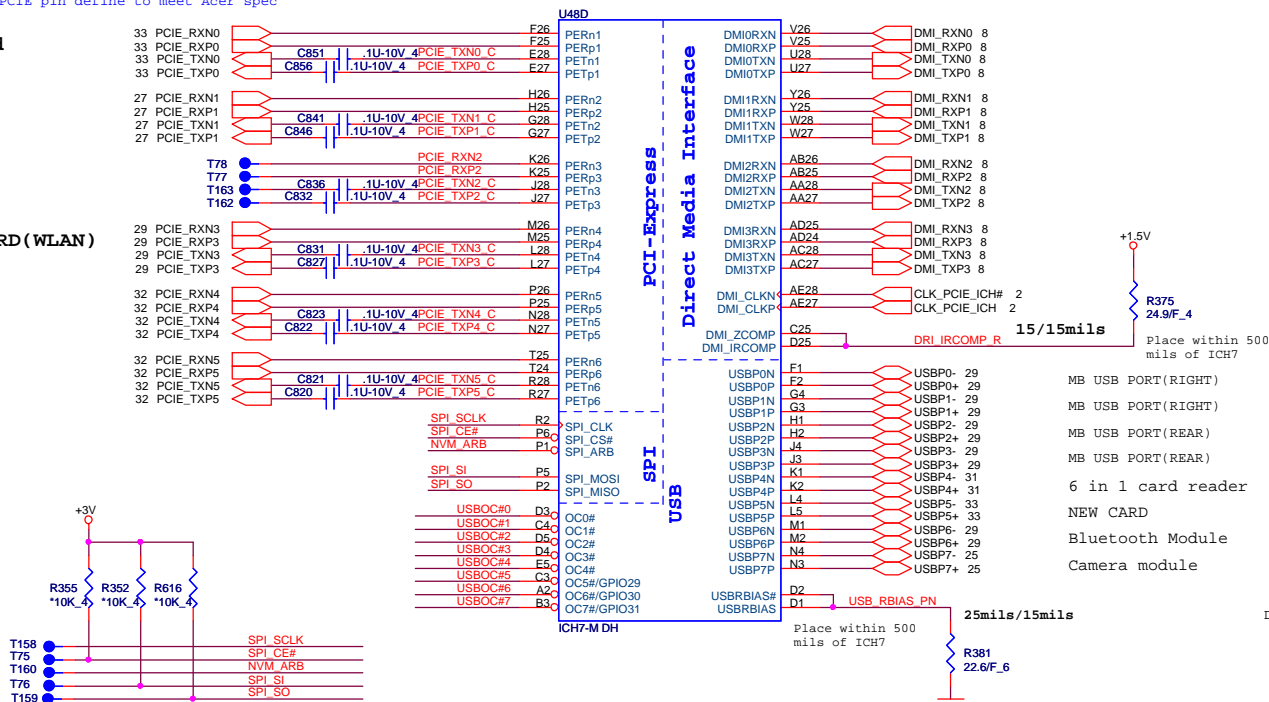
## New card

## GLAN

## MINI CARD(WLAN)

## EZ4\_1

## EZ4\_2



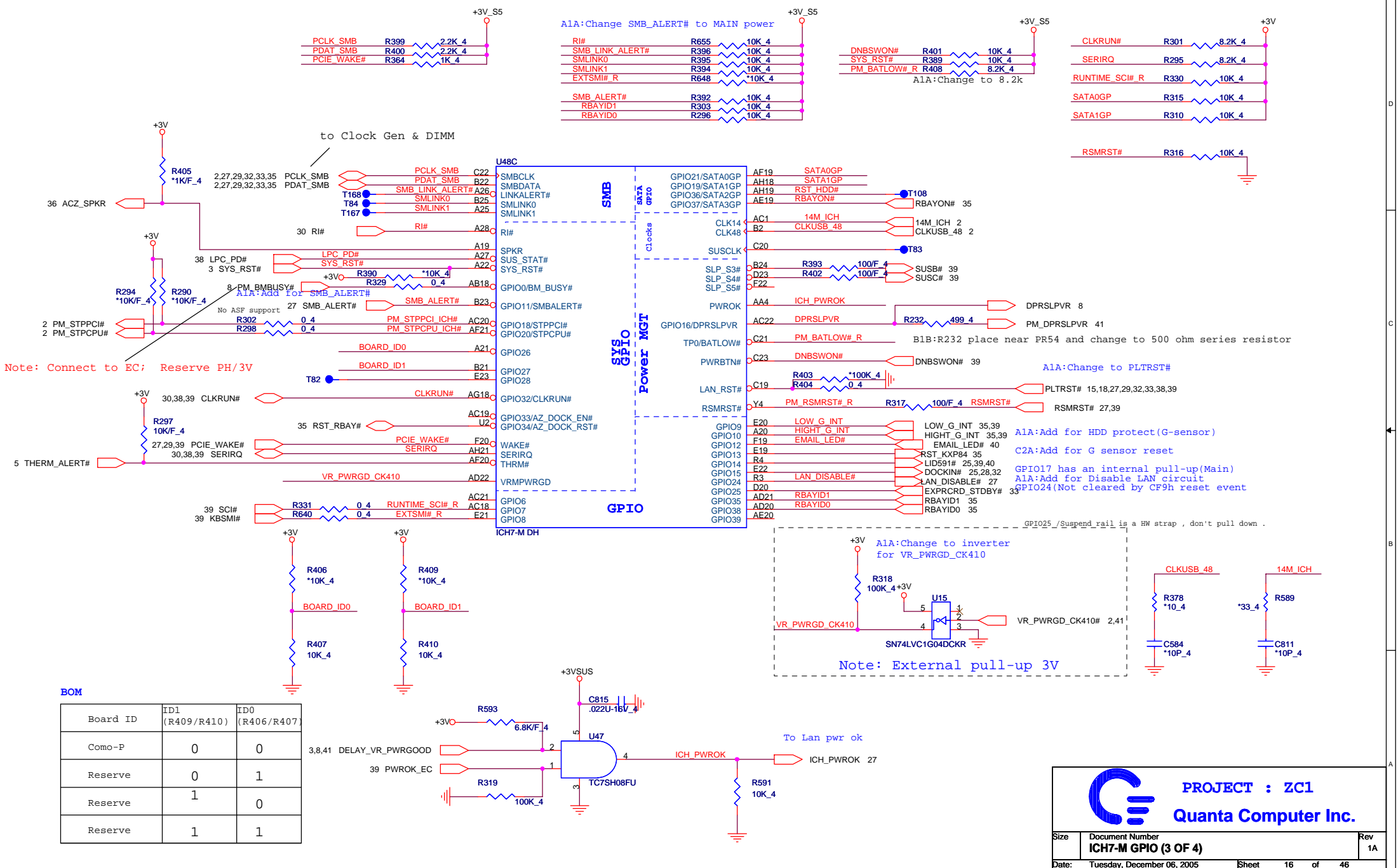
## ICH7 Boot BIOS select

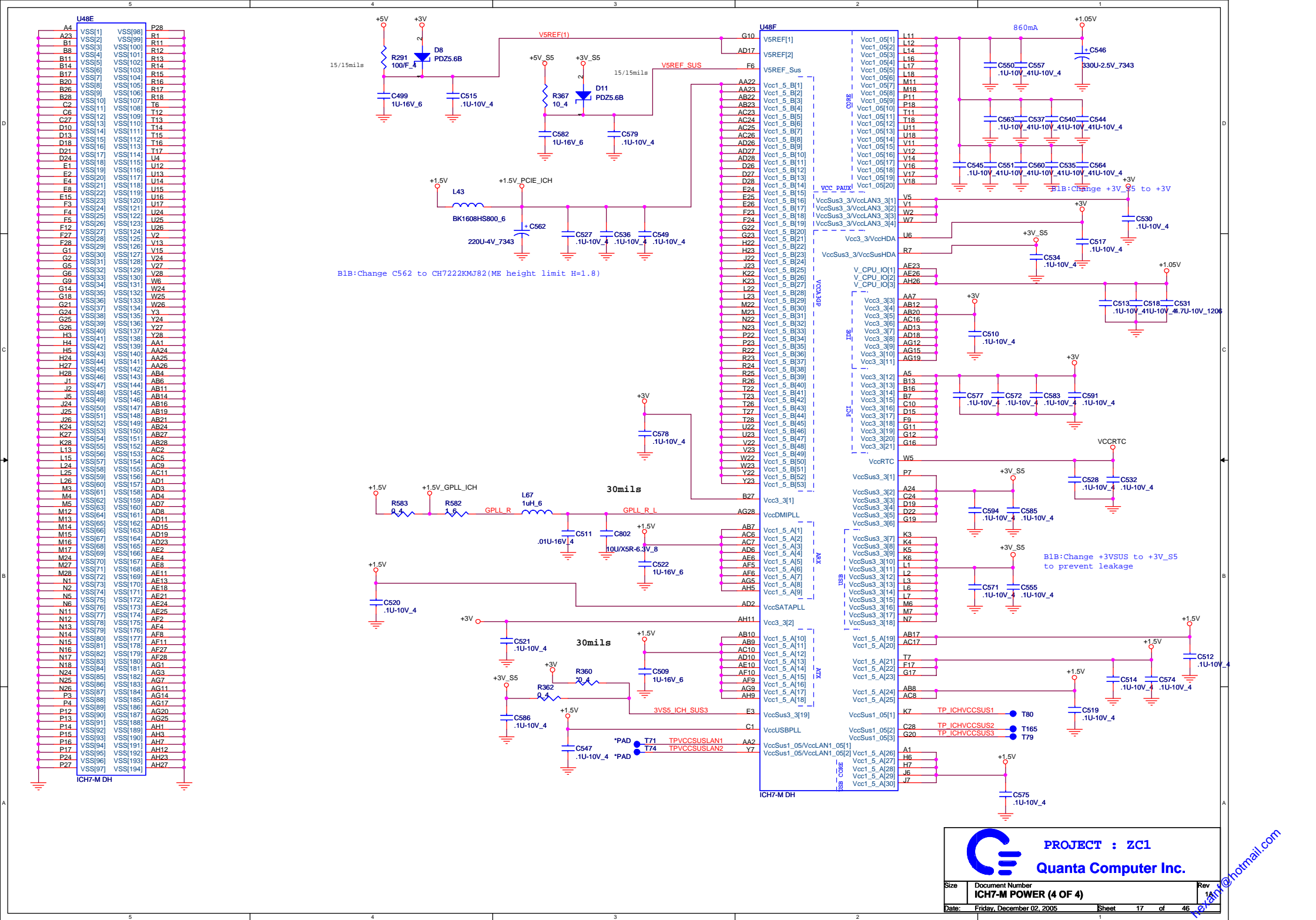
	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
OZ711MP1	AD25	REQ0# / GNT0#	INTE#

**PROJECT : ZC1**  
**Quanta Computer Inc.**

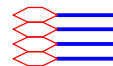
Don't connect to PCI device / Express card



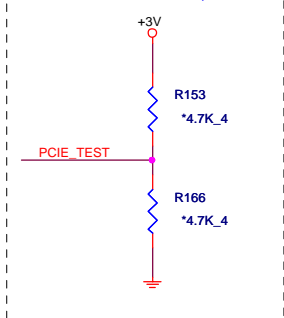


PCIE TEST PADS  
PCIE TEST POINTS MUST BE WITHIN 250 MILS  
OF THE ASIC BALL WITH POSITIVE AND NEGATIVE  
SIGNALS THE SAME DISTANCE

8 PEG\_RXP[15:0]  
8 PEG\_RXN[15:0]  
8 PEG\_TXP[15:0]  
8 PEG\_TXN[15:0]

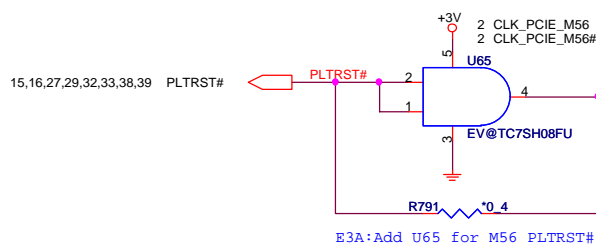
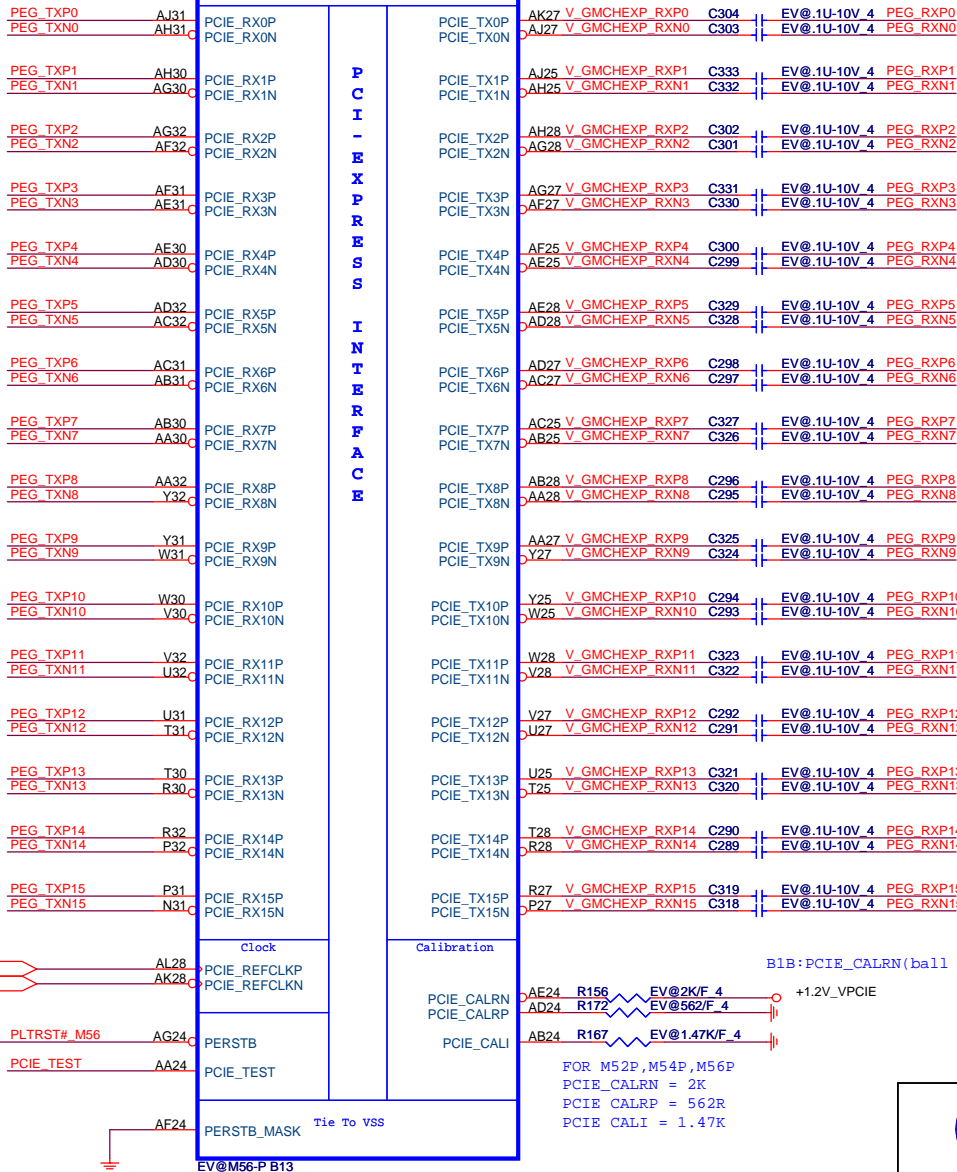


ATI FEATURE NOT ENABLED (M52P,M54P,M56P)  
B1B:Don't stuff R153,R166 for PCIE\_TEST

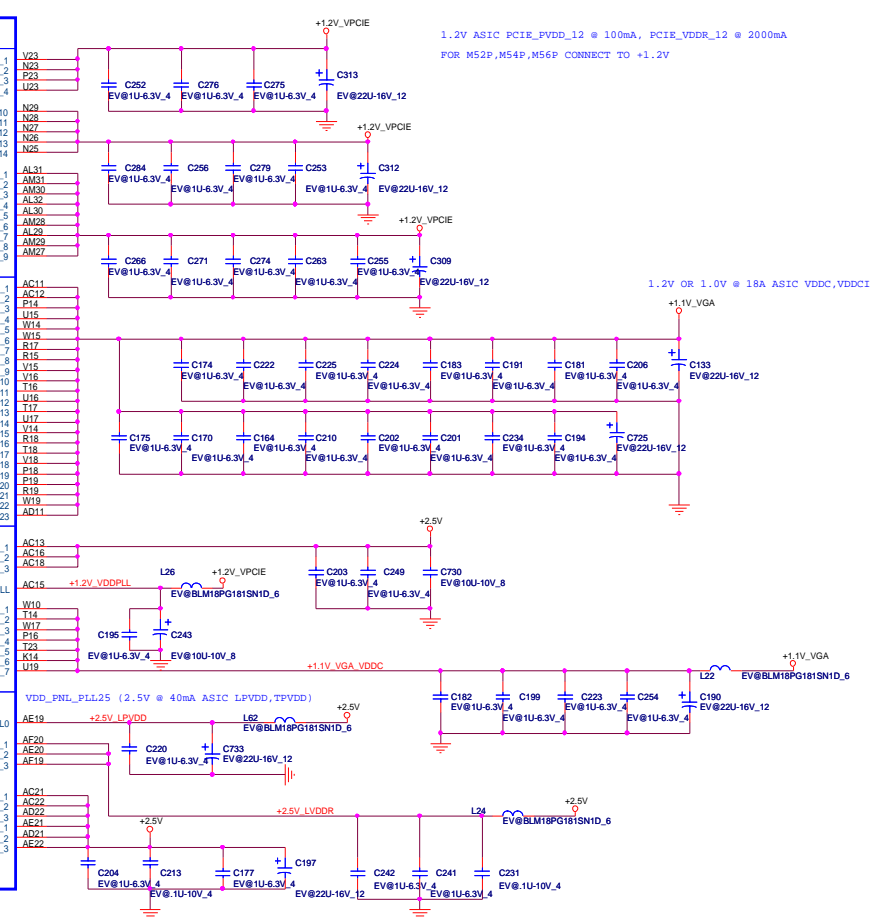
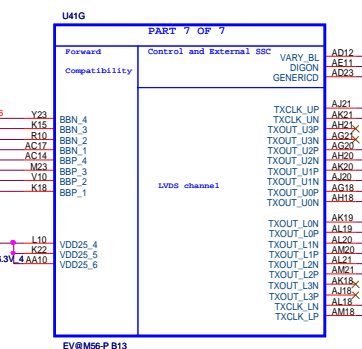
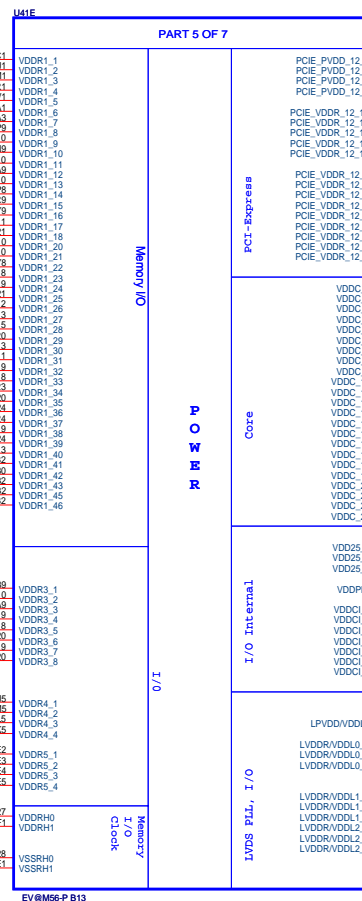
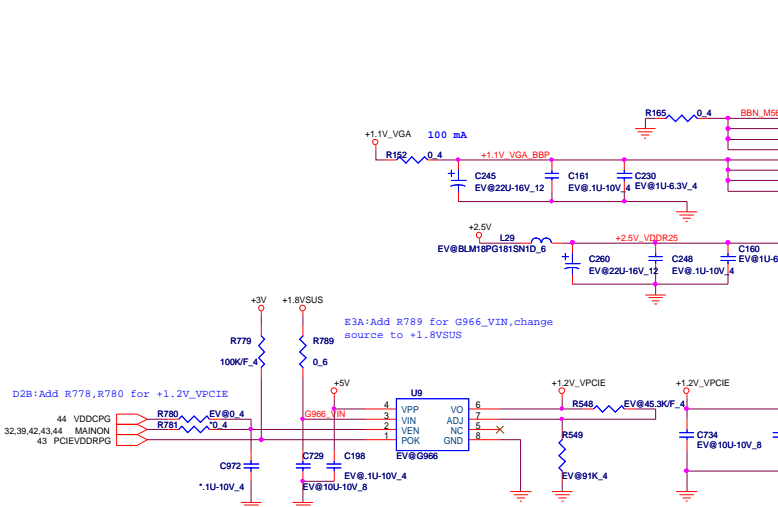
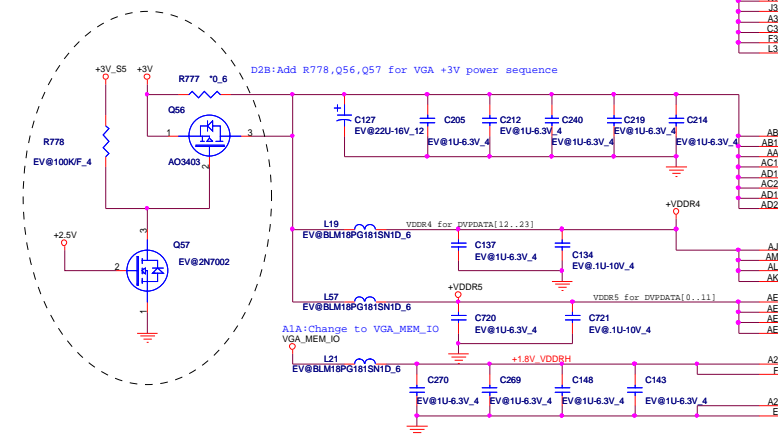


U41A

PART 1 OF 7

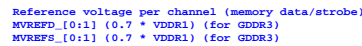




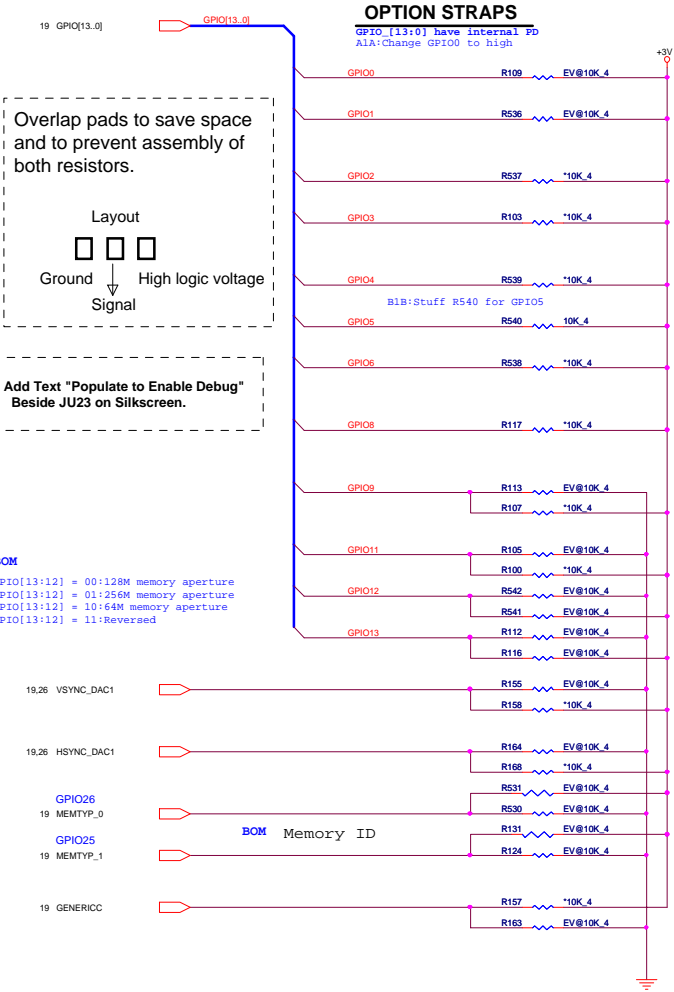




### Channel B







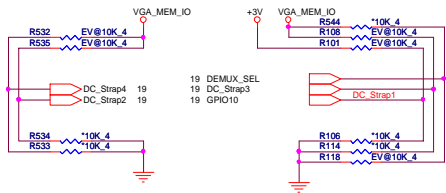
M56-P Strap

STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE FOR M26X,M50P: INSTALL WITH ATI R3480,R3490,R3490,R3490, R3410,R3480,CHIPSETS DO NOT INSTALL WITH INTEL 915PM CHIPSET FOR M5X - INSTALL	TBD
RSVD	GPIO(3:2)	NO ATI FEATURE ENABLED	DO NOT INSTALL 10K RESISTORS
REVERSE LANES DEBUG ACCESS	GPIO4	NO DEBUG ACCESS (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE RSVD	GPIO5	sets the desired PCIE PLL bandwidth for M5x parts	DO NOT INSTALL 10K RESISTOR
COMMON MODE RANGE	GPIO6	NO ATI FEATURE ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
DEBUG ACCESS FORCE_COMPLIANCE	GPIO8	DON'T FORCE COMPLIANCE STATE(M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
ROMIDCFG(3:0) MEMORY APERTURE SIZE	GPIO(8,13:11)	IF NO ROM GPIO11(M26X) AND GPIO12,13(M52,M54,M56) SET MEMORY APERTURE SIZE 000x - No ROM, MEM_AP_SIZE=0(128MB) 001x - No ROM, MEM_AP_SIZE=0(256MB) 010x - No Rom, MEM_AP_SIZE=10(64MB) 011x - No ROM, MEM_AP_SIZE=11(Reserved) 1000 - Parallel ROM, chip IDs from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDs from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDs from ROM 1011 - Serial M25P10 ROM (ST), chip IDs from ROM 1100 - Serial M25P05 ROM (ST), chip IDs from ROM 1100 - Serial NX25F0118 ROM (SSD), chip IDs from ROM	A1A:change ROMIDCFG(3:0) to 0010
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0 - Slave VIP host port device present. 1-No slave VIP port devices reporting presence during reset	No default
NO STRAP FUNCTION	H2SYNCR, V2SYNCR,GENERICC	ATI FEATURE NOT ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
	VSYNC	RSVD	
	HSYNC	RSVD	
	PCIE_TEST	RSVD	

Board Straps

REV 0.3

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYP(1:0)	GPIO25,26	MEMORY TYPE AND SPEED SELECT Memory connected to R420 identification for BIOS 00 - Samsung GDDR 3 memory(256Mb) 136 Ball BGA package 01 - Samsung GDDR 3 memory(512Mb) 136 Ball BGA package 10 - Infineon GDDR 3 memory(256Mb) 136 Ball BGA package 11 - Infineon GDDR 3 memory(512Mb) 136 Ball BGA package	00
DC_Strap1	GPIO(10)	Internal TMS Enabled 0 - Disabled 1 - Enabled	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled 0 - Disabled 1 - Enabled	1
DC_Strap3	LCDDATA(14)	HDTV out detect 0 - Detected 1 - Not detected	1
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off 01 - DAC2 On as CRT 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	10
PALNTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 - NTSC (on board resistor pull-up)	1

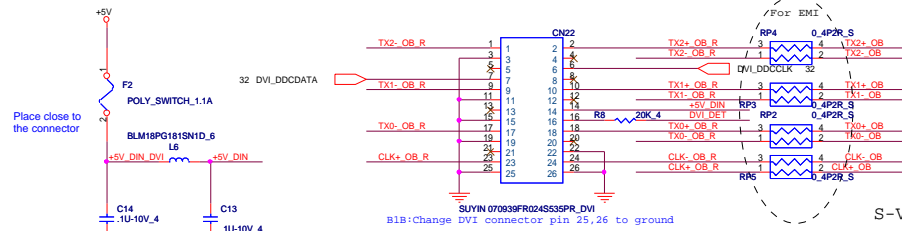


A1A:change video capture  
enable setting

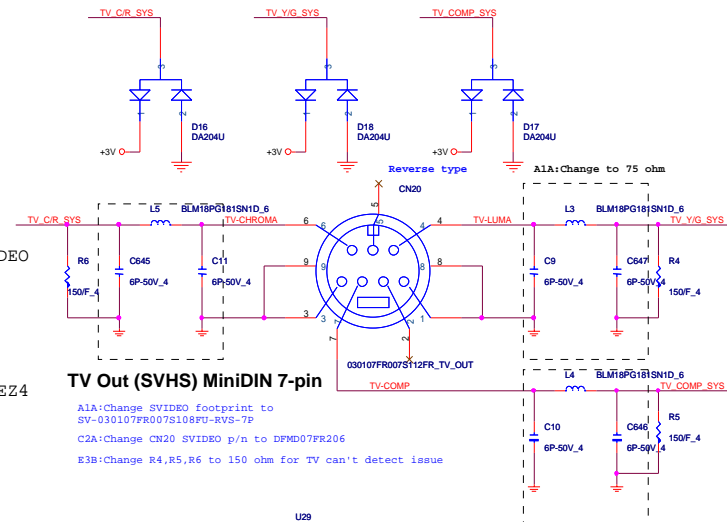
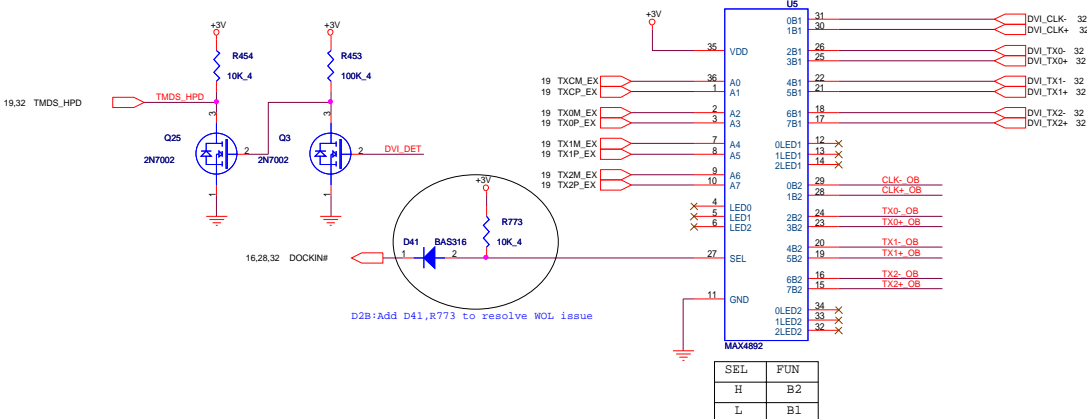


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# DVI-I CONNECTOR (DVI-D)

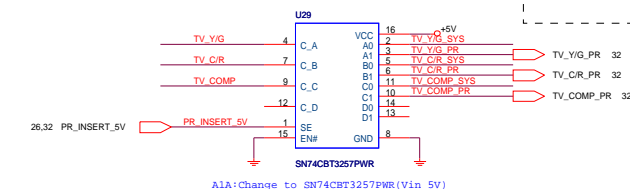


## DVI PORT

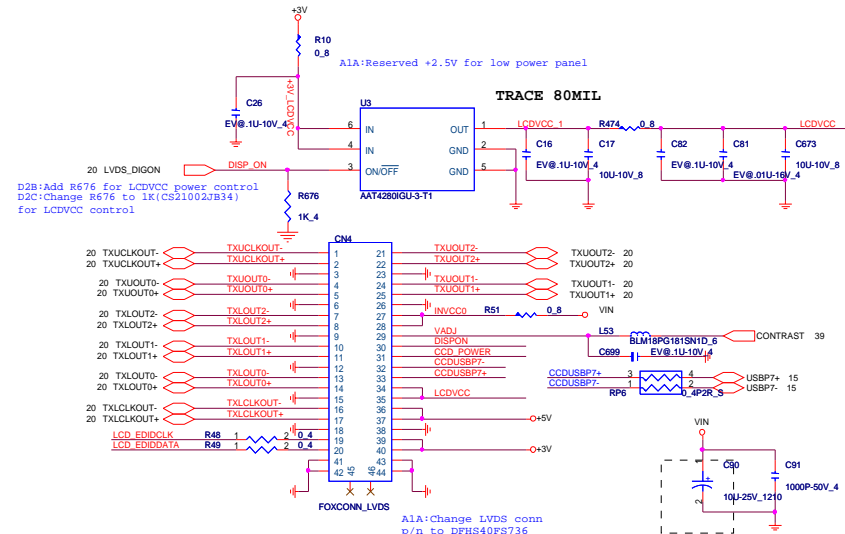
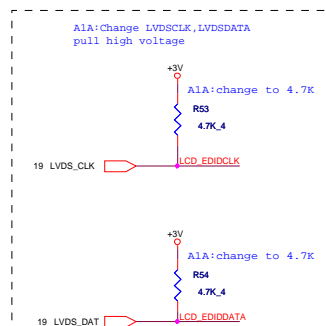
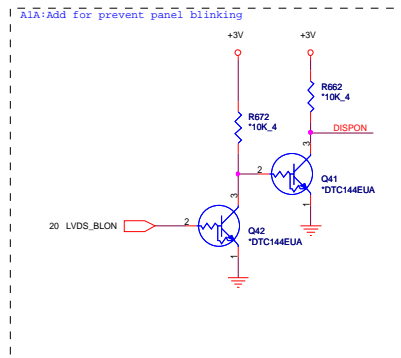
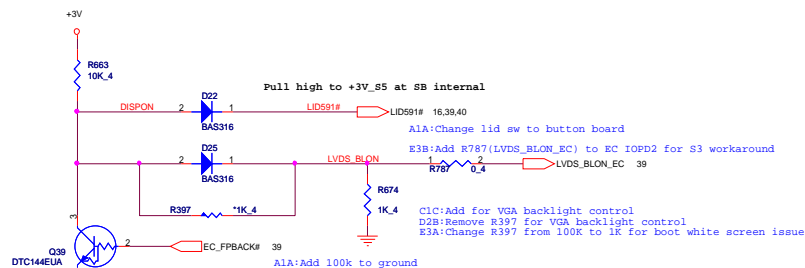


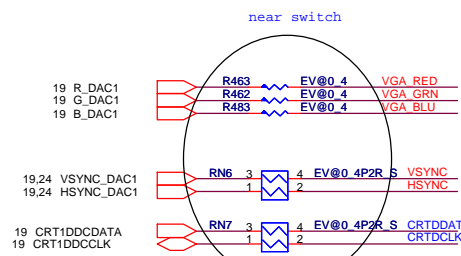
## TV Out (SVHS) MiniDIN 7-pin

A1A:Change SVIDEO footprint to SV-030107FR007S112FR-RVS-7P  
C2A:Change CN20 SVIDEO p/n to DFMD07FR206  
E3B:Change R4,R5,R6 to 150 ohm for TV can't detect issue

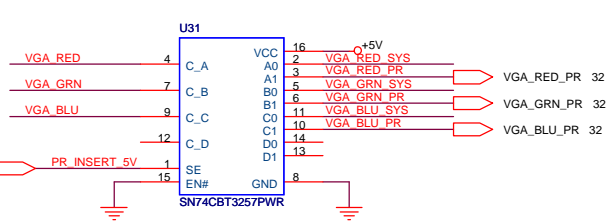


19\_Y\_DAC2 EV@0.4 TV\_YIG  
19\_C\_DAC2 EV@0.4 TV\_CIR  
19\_COMP\_DAC2 EV@0.4 TV\_COMP





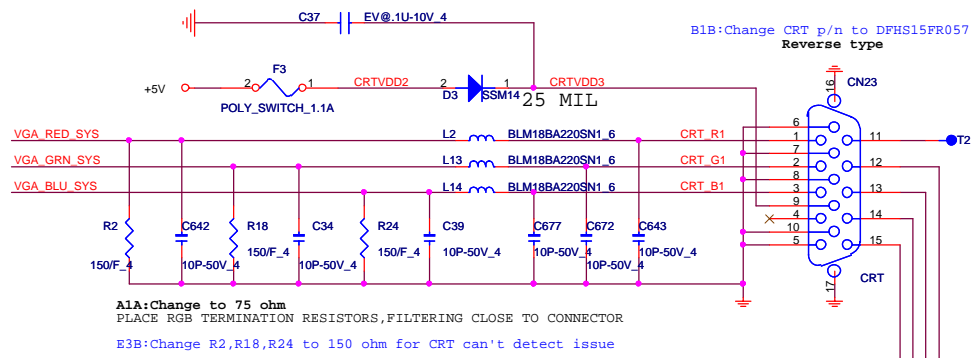
25,32 PR\_INSERT\_5V



A1A:Change to SN74CBT3257PWR(Vin 5V)

SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

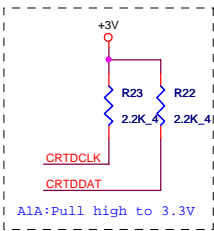
B1B:Remove UMA CRT support



A1A:Change to 75 ohm  
PLACE RGB TERMINATION RESISTORS, FILTERING CLOSE TO CONNECTOR  
E3B:Change R2,R18,R24 to 150 ohm for CRT can't detect issue

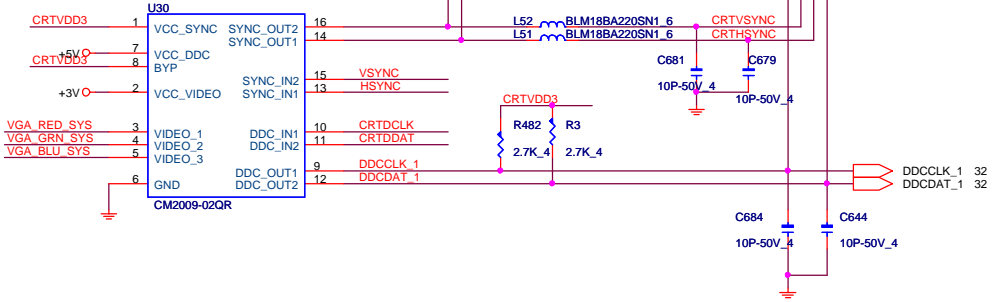
B1B:Change CRT p/n to DFHS15FR057  
Reverse type

A1A:delete CRT\_SENSE#

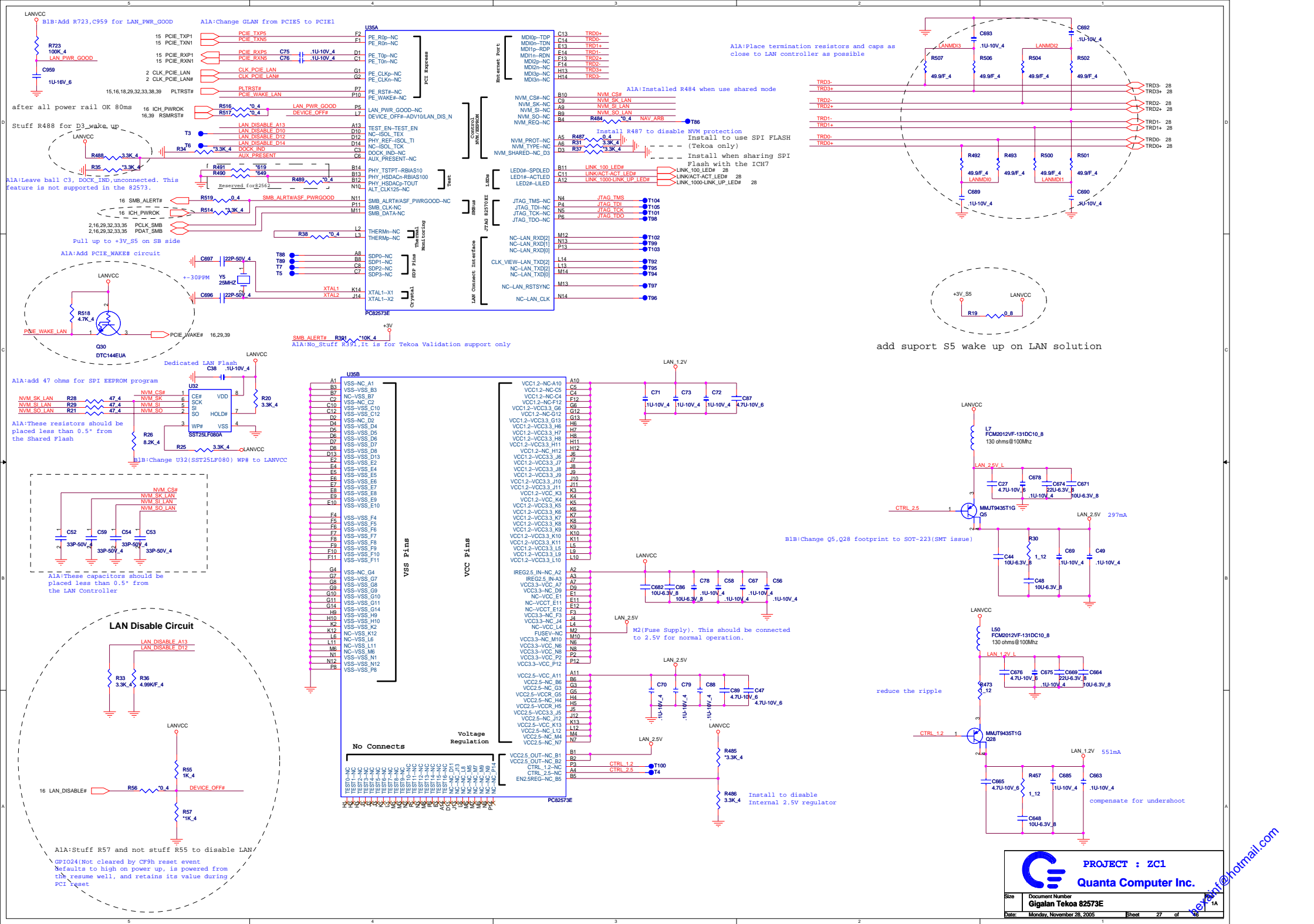


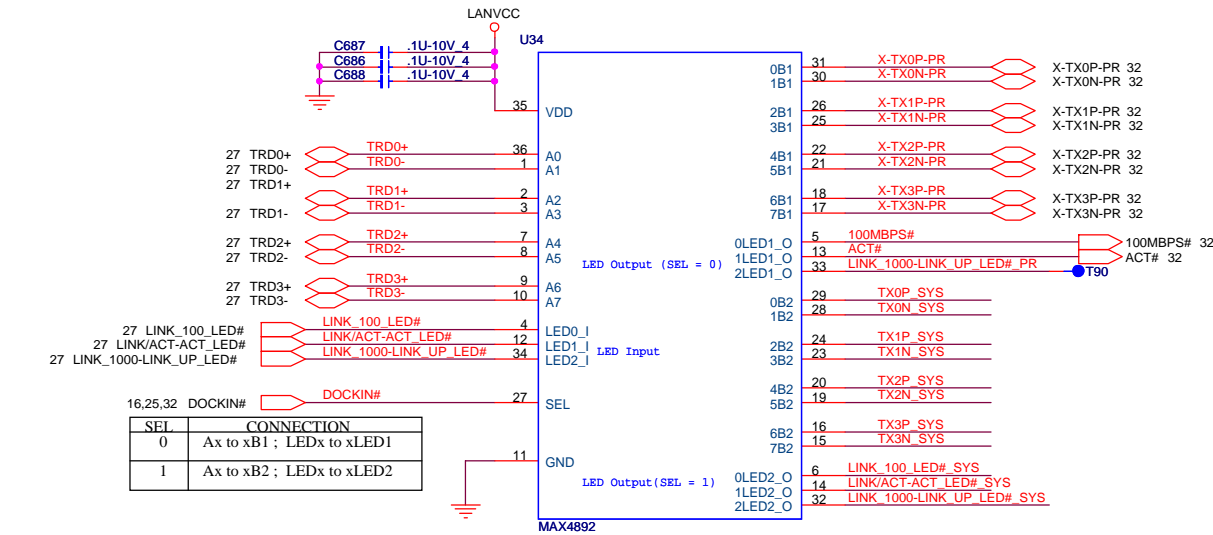
A1A:Pull high to 3.3V

B1B:Change U30 pin1,8,9,12 to CRTVDD3



PROJECT : ZC1  
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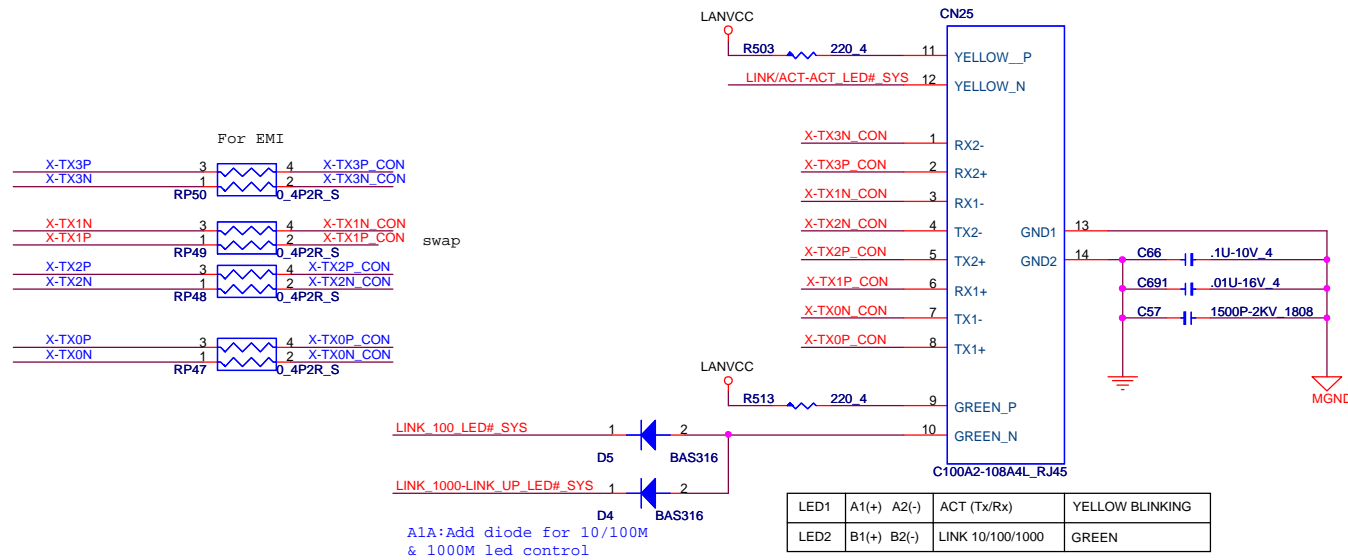




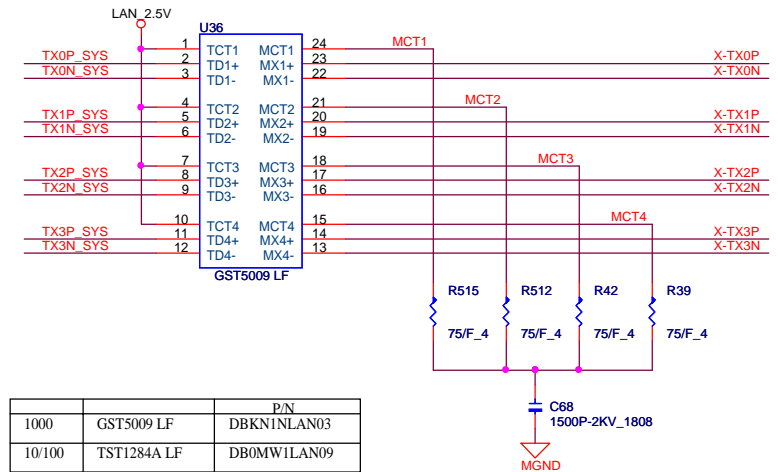
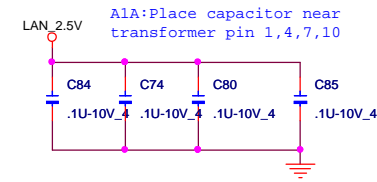
LED0 Input  
 0LED1 Output. Connects LED0 to 0LED1 when SEL = 0.  
 0LED2 Output. Connects LED0 to 0LED2 when SEL = 1.

B1B:Change MAX4892 pin define

A1A:Change RJ45 CONN to C100A2-108A4L  
 A1A:Change RJ45 TX,RX pin define



LED1	A1(+)	A2(-)	ACT (Tx/Rx)	YELLOW BLINKING
LED2	B1(+)	B2(-)	LINK 10/100/1000	GREEN



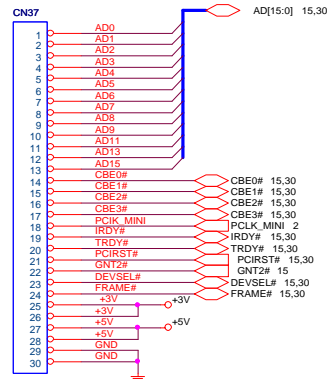
		P/N
1000	GST5009 LF	DBKN1NLAN03
10/100	TST1284A LF	DB0MW1LAN09

**PROJECT : ZC1**  
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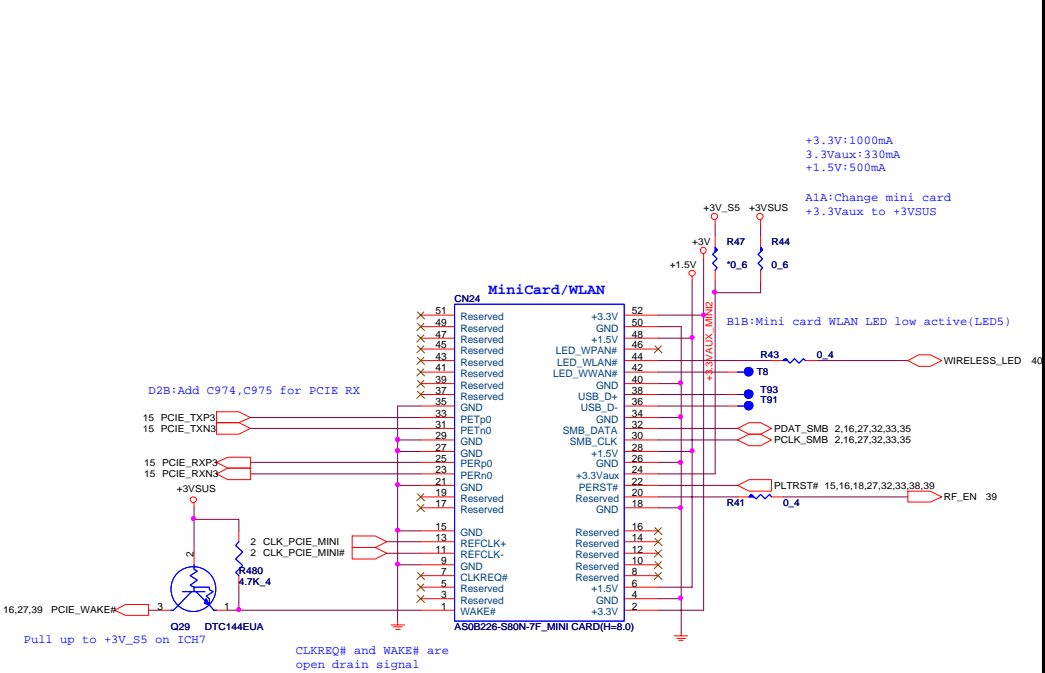
Size	Document Number	Rev
	<b>TRANSFORMER/RJ45</b>	<b>A</b>
Date:	Monday, November 28, 2005	Sheet 28 of 46

# Debug card interface

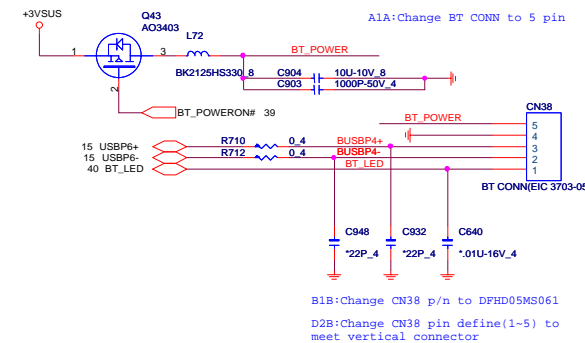
BT contact



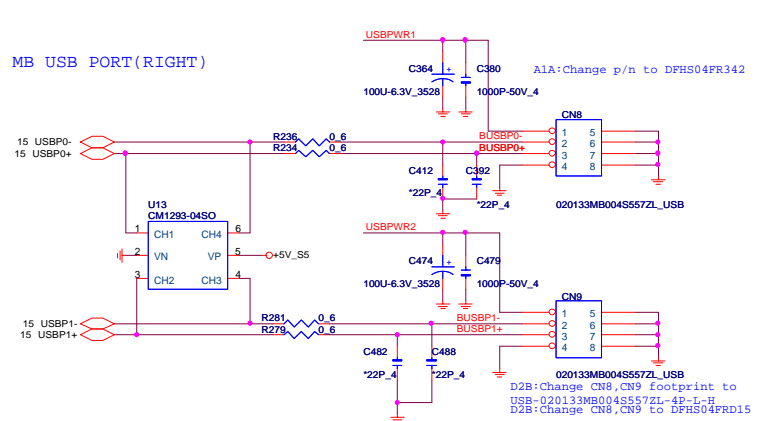
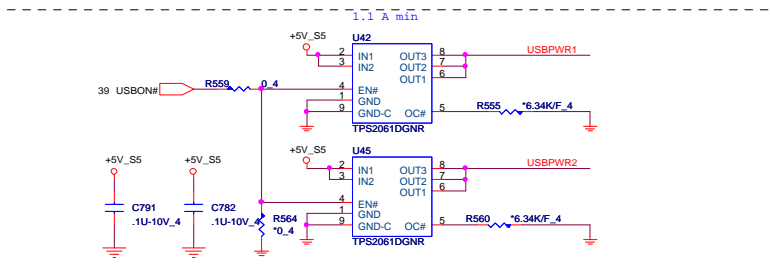
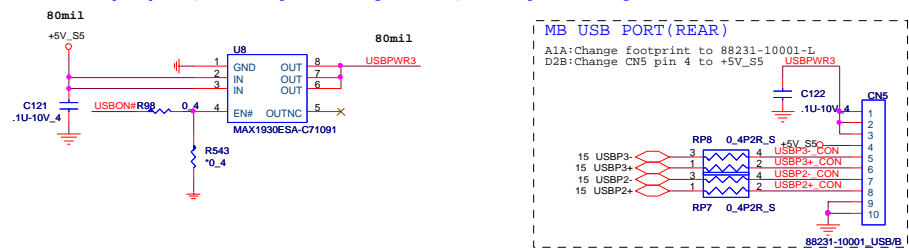
AFN300-N2G1Z\_DEBUG



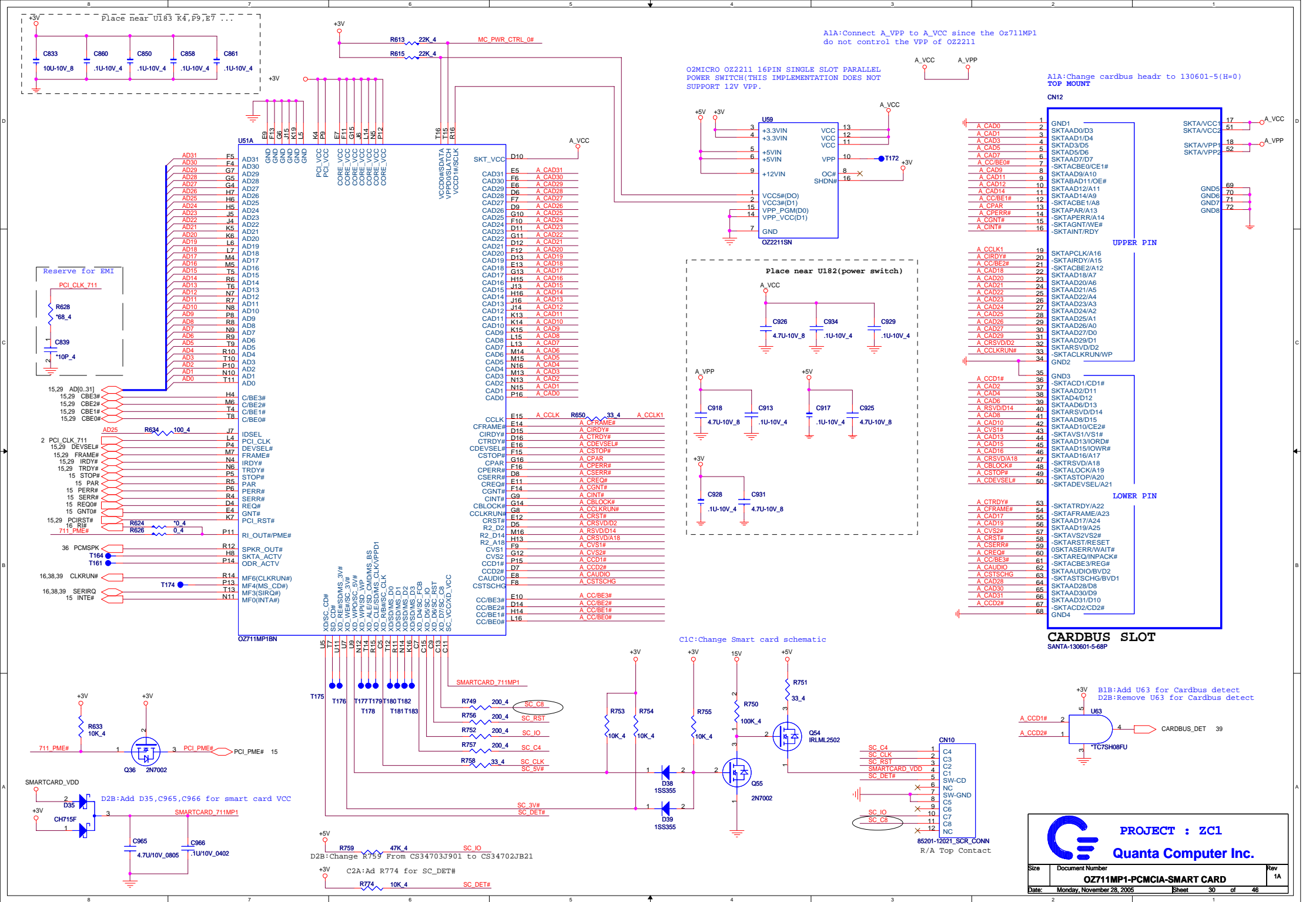
# BLUETOOTH MODULE CONNECTOR

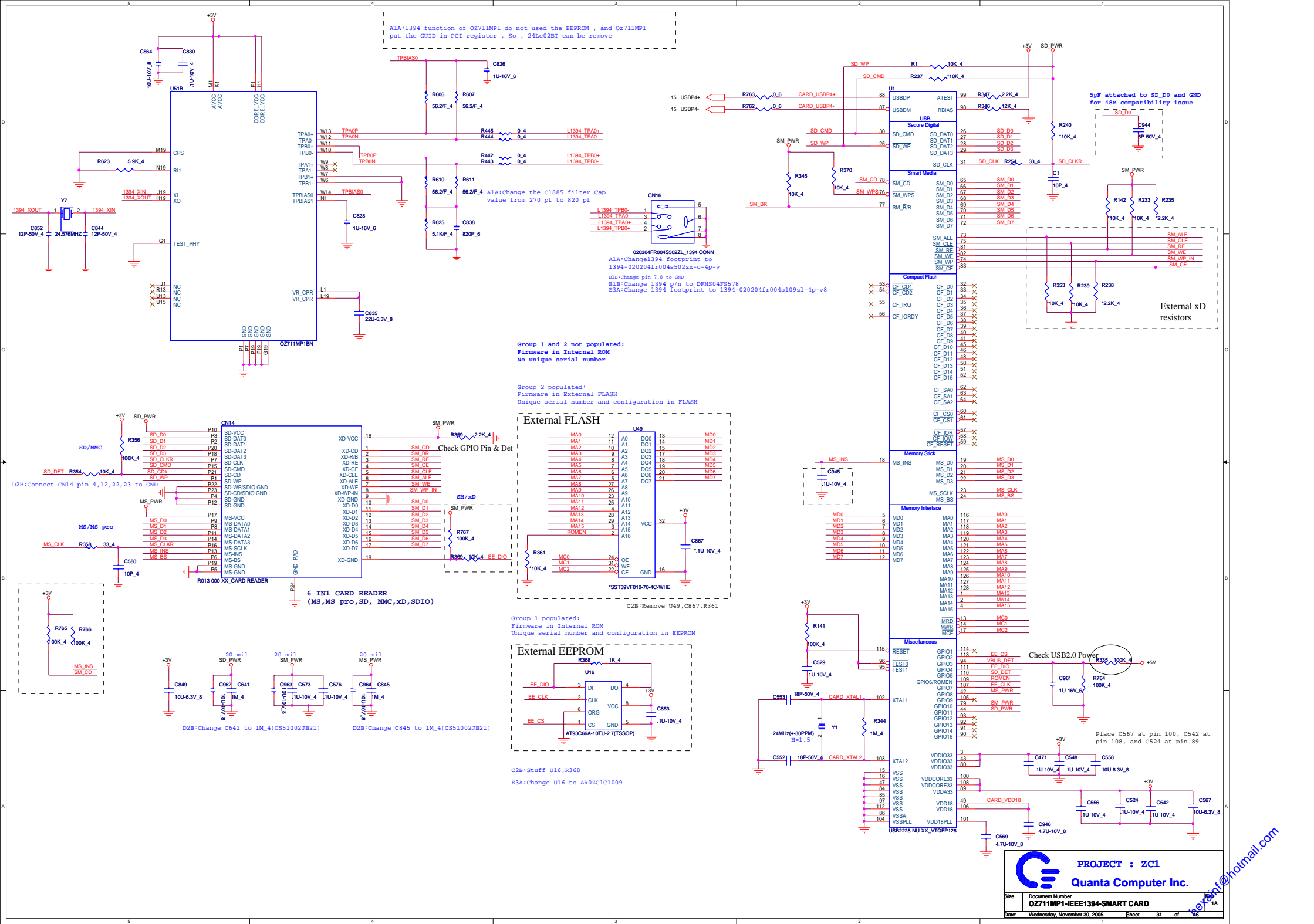


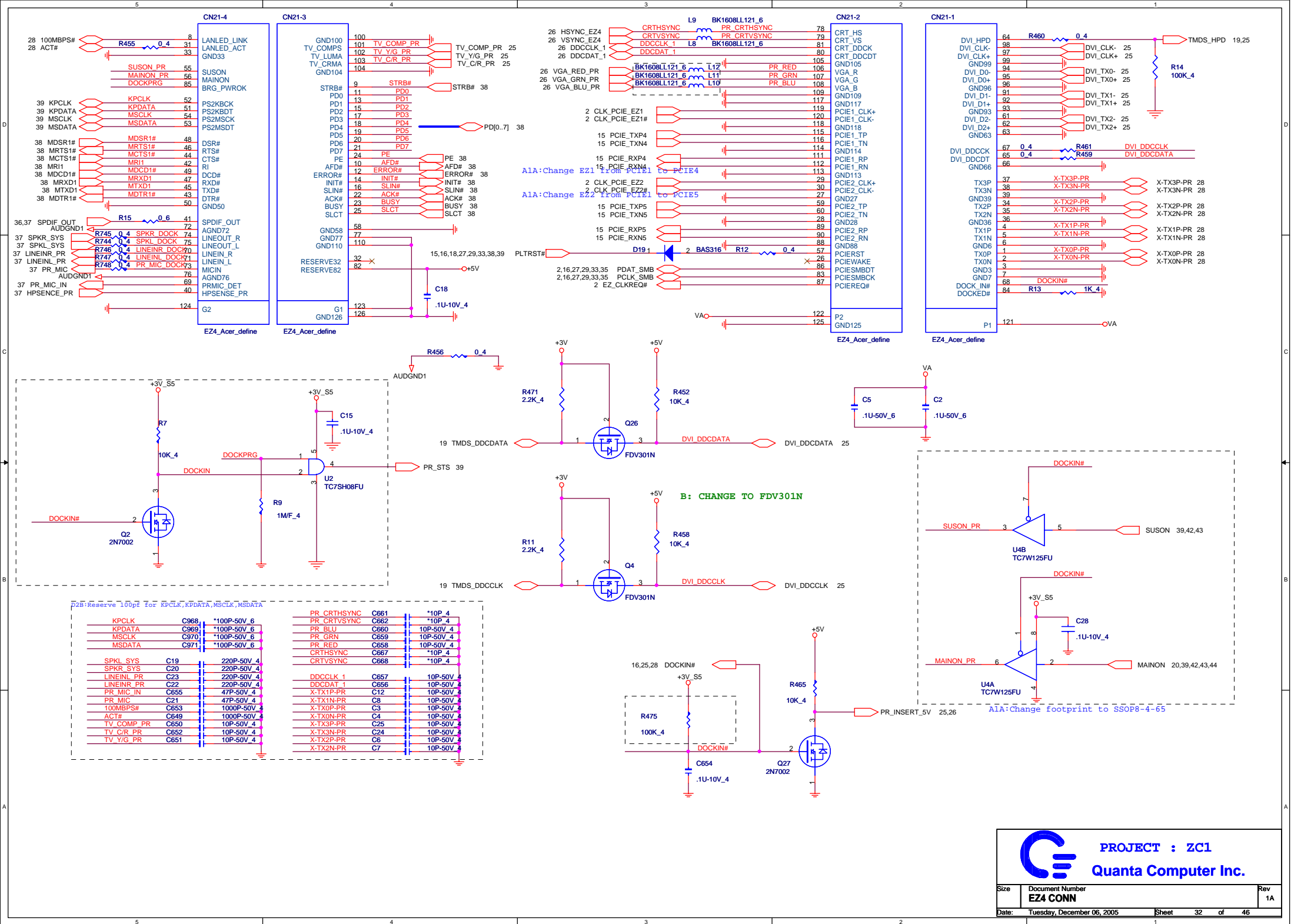
A1A:In adapter mode, should be powered during S0-S5.  
In battery only mode, should be powered during S0 and S3, and not powered during S5



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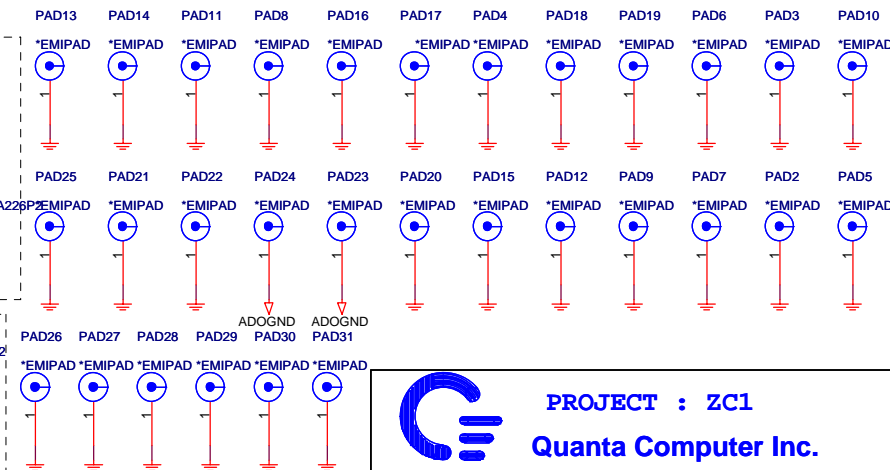
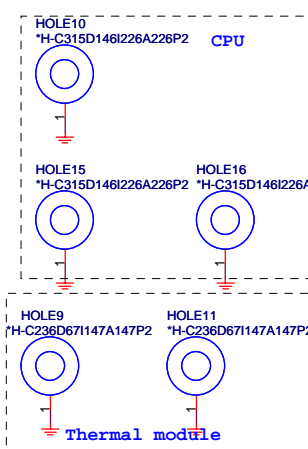
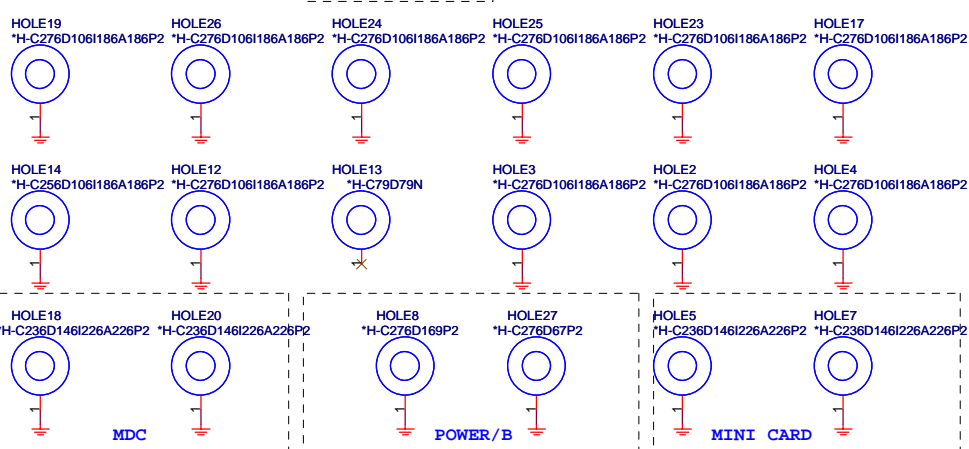
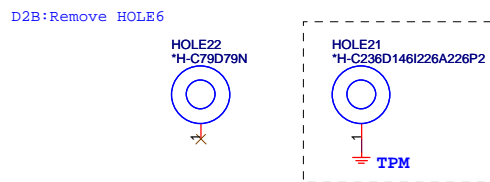
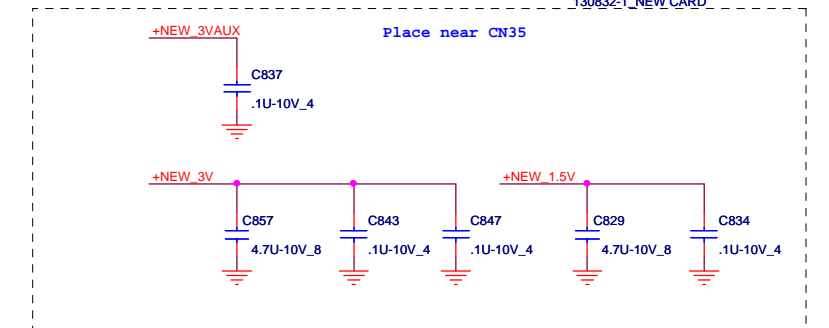
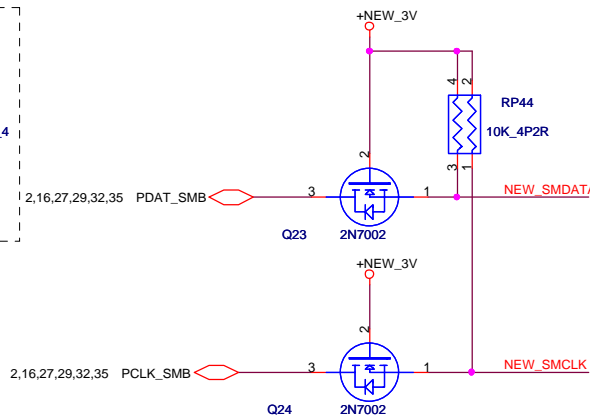
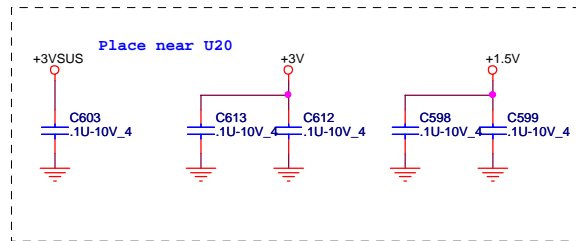
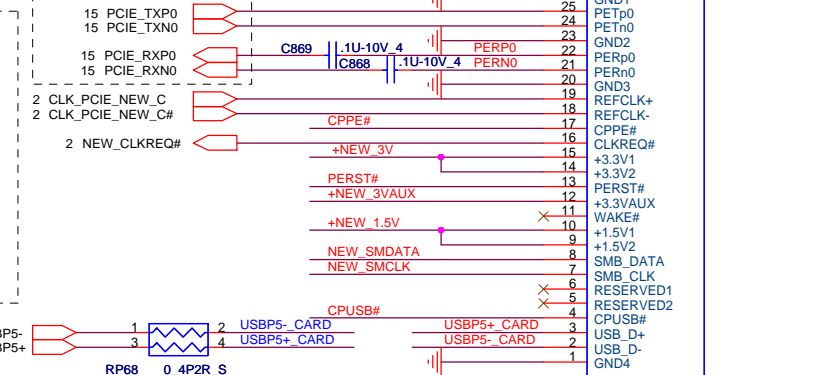
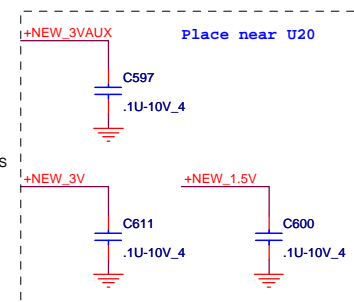
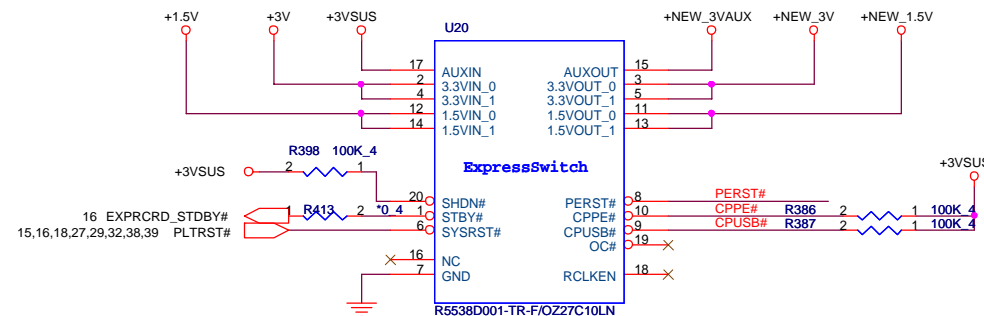






+NEW\_1.5V Max. 650mA, Average 500mA.  
+NEW\_3V Max. 1300mA, Average 1000mA.

A1A:Change New card power sw to Oz27c10



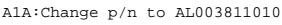
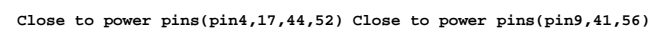
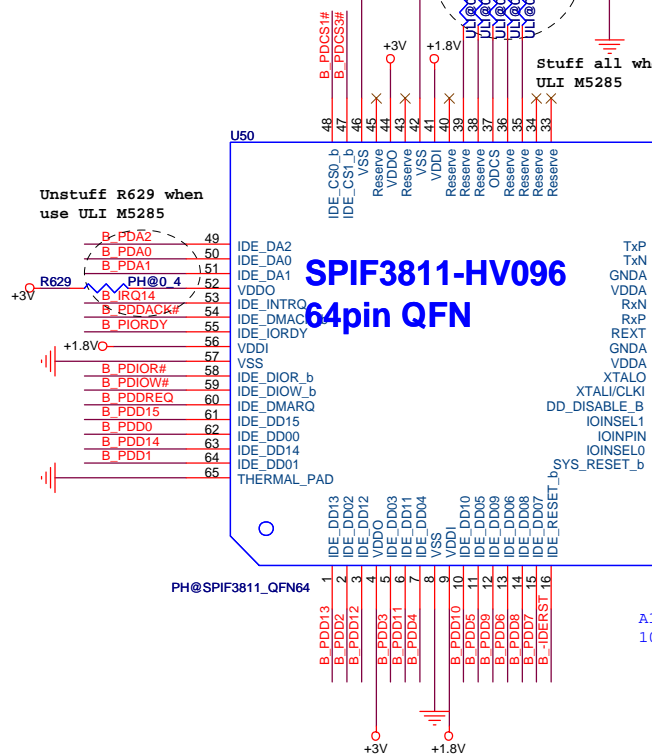
B1B:Change HOLE8,27 footprint

**PROJECT : ZC1**  
**Quanta Computer Inc.**

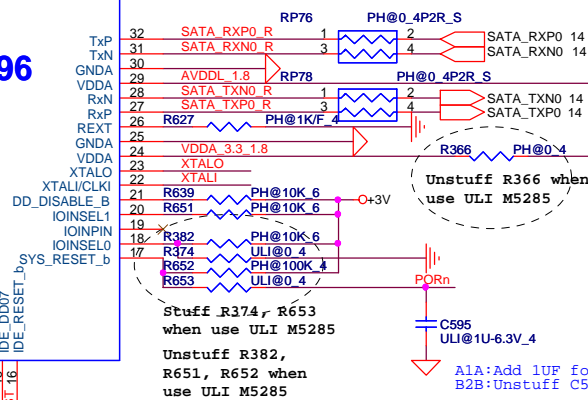
Size	Document Number	Rev
	<b>NEW CARD &amp;HOLE</b>	C
Date:	Monday, November 28, 2005	Sheet 33 of 46

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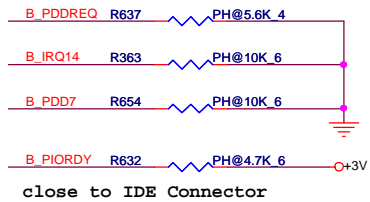
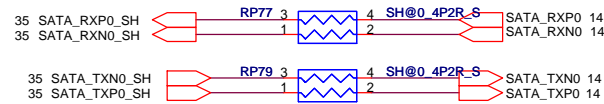
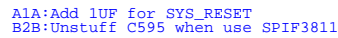
## SATA TO PATA



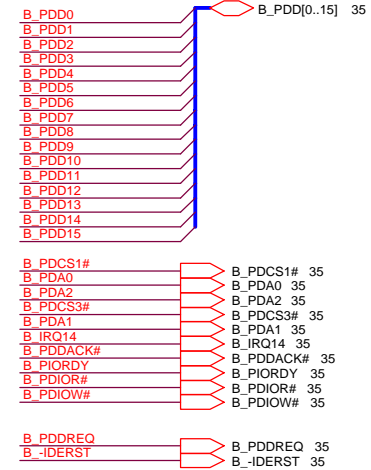
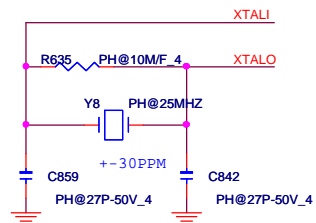
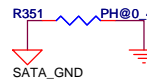
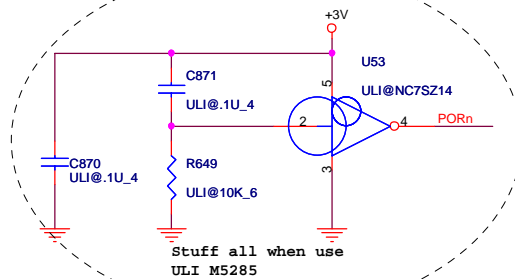
SATA AC coupling is 0.01UF



```
A1A:Change Pin 21 (DD_DISABLE#)
10K ohm  PU to  +3.3V
```



```
1.8 V Supply current for PHY blocks 120 mA
1.8 V Supply current for core logic 90 mA
3.3 V Supply current ( for I/O)      55 mA
```



## Reference clock select

ATAIOEN	Note
0	disable PATA output
1	enable PATA output

### Operation Mode

## Reference clock select

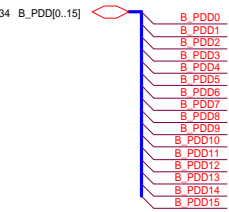
<b>CLKSEL[1..0]</b>	External clock
0 0	20 MHz
0 1	25 MHz



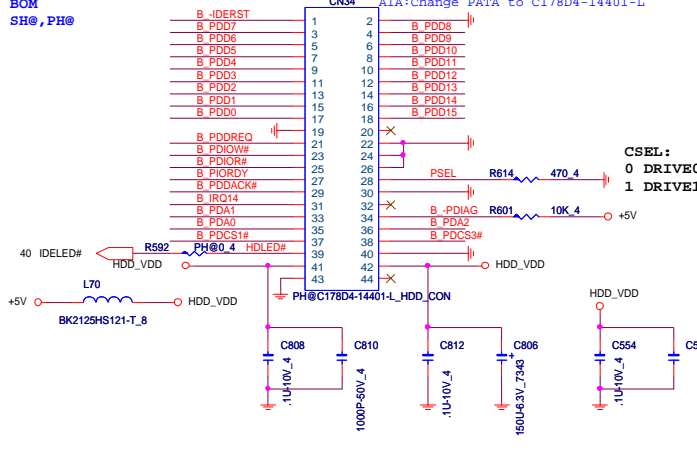
PROJECT : ZC1  
Quanta Computer Inc.

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From SATA -> PATA bridge

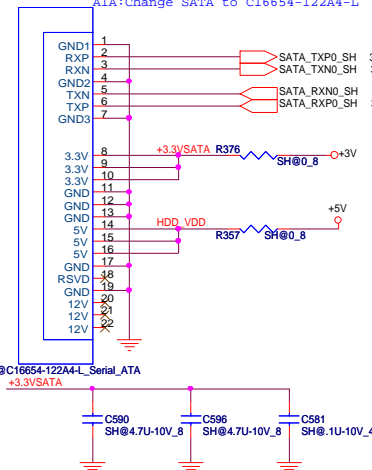


BOM  
SH@,PH@



CSEL:  
0 DRIVE0  
1 DRIVE1

A1A:Change SATA to C16654-122A4-L



+3VSUS +3V

R736 0.4  
R722 0.4

KXP84\_VDD

C464 C466

4.7U-10V\_8 1U-10V\_4

16.39 HIGHT\_G\_INT

16.39 LOW\_G\_INT

C473 C476 C481

0.02U-16V\_4 0.02U-16V\_4 0.02U-16V\_4

Bandwidth control(#50HZ)

KXP84\_VDD

ADDRO

R255 10K\_4

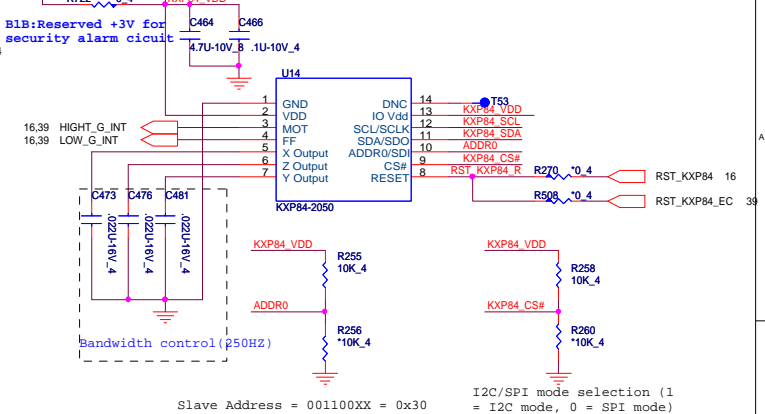
R256 10K\_4

Slave Address = 001100XX = 0x30

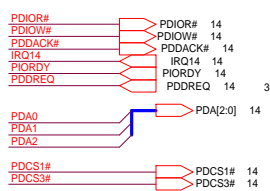
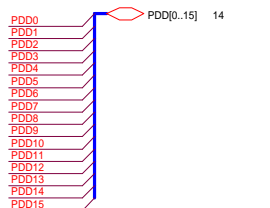
I2C/SPI mode selection (1 = I2C mode, 0 = SPI mode)

A1A:Add for HDD protect(G-sensor)

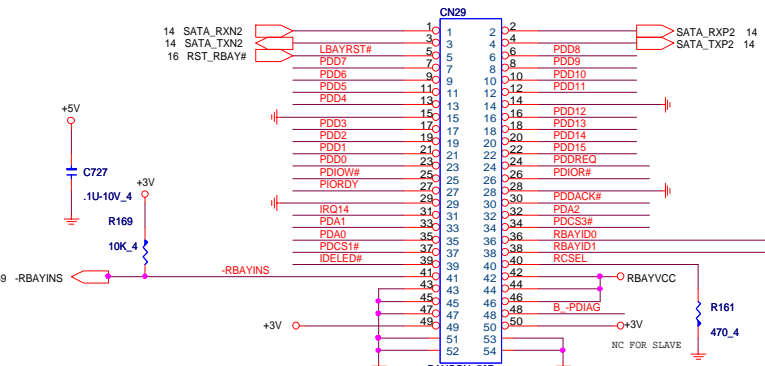
E3B:Change U14 to KXP84-2050(new version IC)



From ICH7 bridge



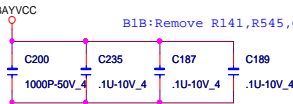
Media Bay Connector



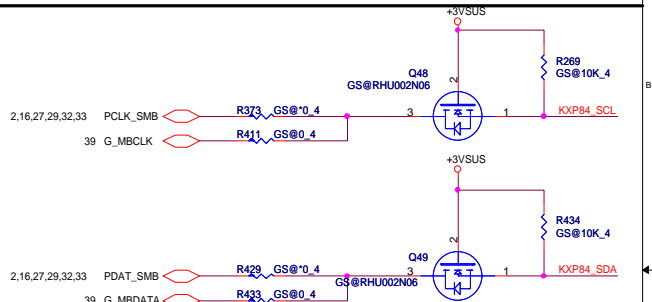
A1A:change -PDIAG to B-PDIAG  
C2A:Stuff R161,set ODD to Master  
C2A:Remove R173 for RBAYID

BAY ID STATUS

RBAYID0/ LBAYID0	RBAYID1/ LBAYID1	STATUS
0	0	FDD
0	1	HDD
1	0	CD/DVD

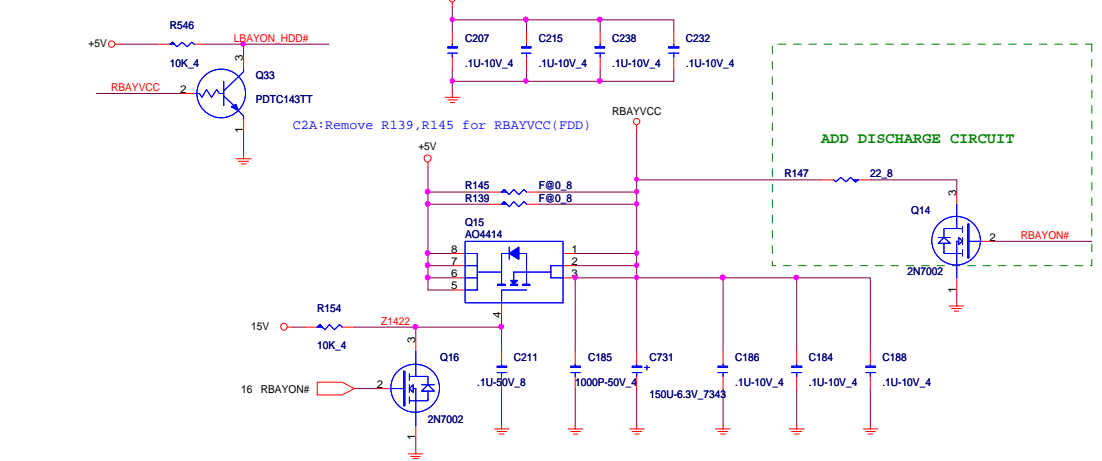
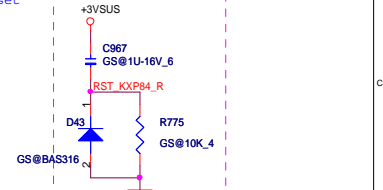


B1B:Remove R141,R545,Q32 for -IDERST



B1B:Add MOS for G sensor SMBUS  
D2B:Change Q48,Q49 VCC to +3VSUS  
D2B:Add R269,R434 for SMBUS PU resistor  
D2B:Add R411,R433 for SMBUS

D2B:Add C967,R775,D43 for G sensor reset



ADD DISCHARGE CIRCUIT

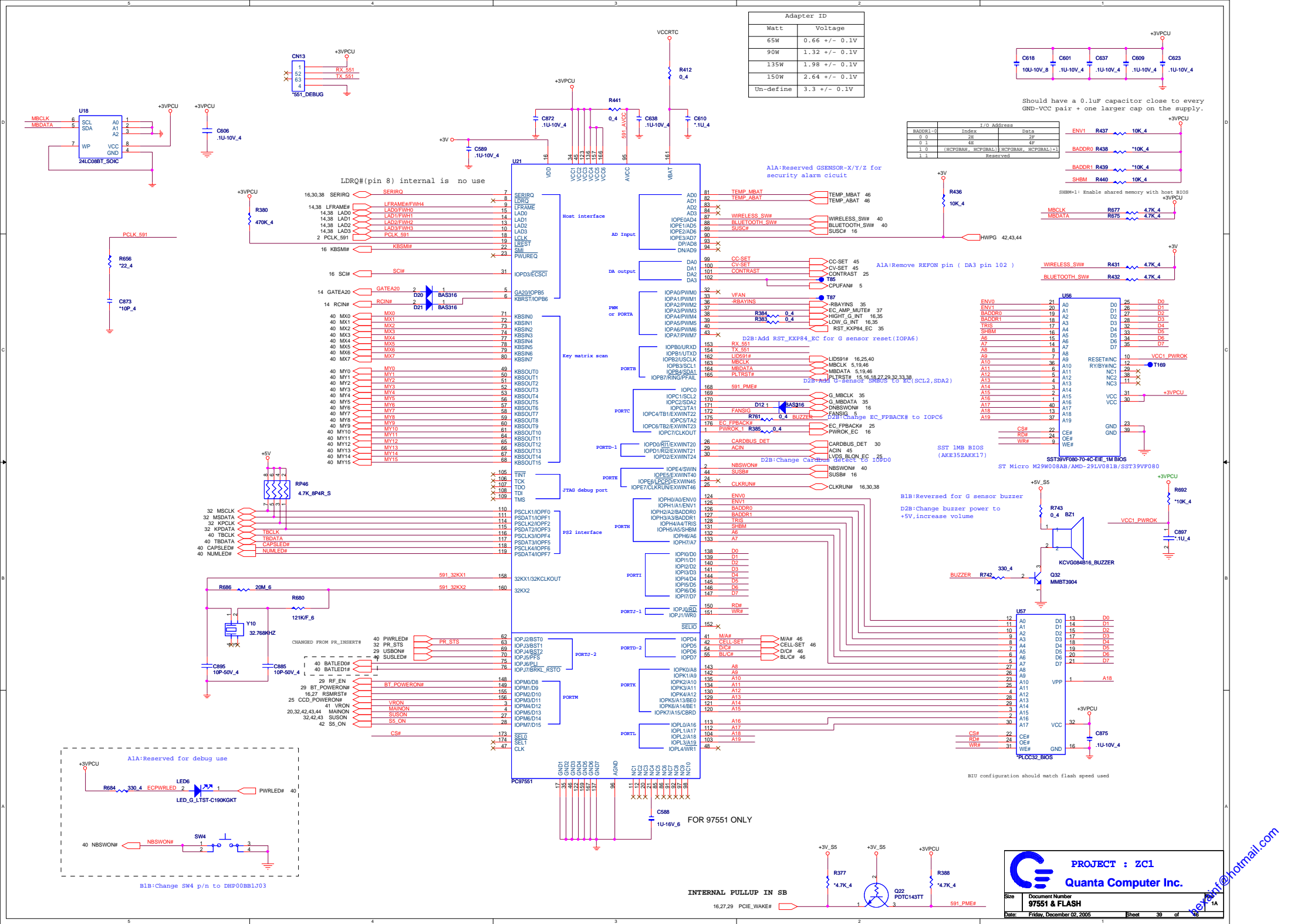
PROJECT : ZC1  
Quanta Computer Inc.

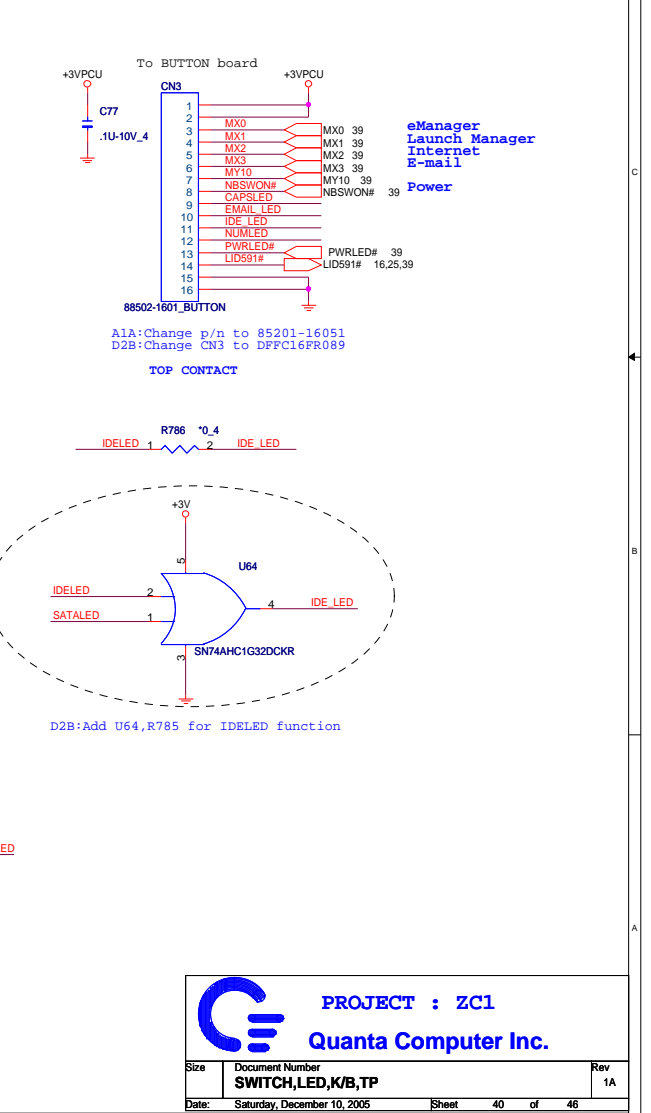
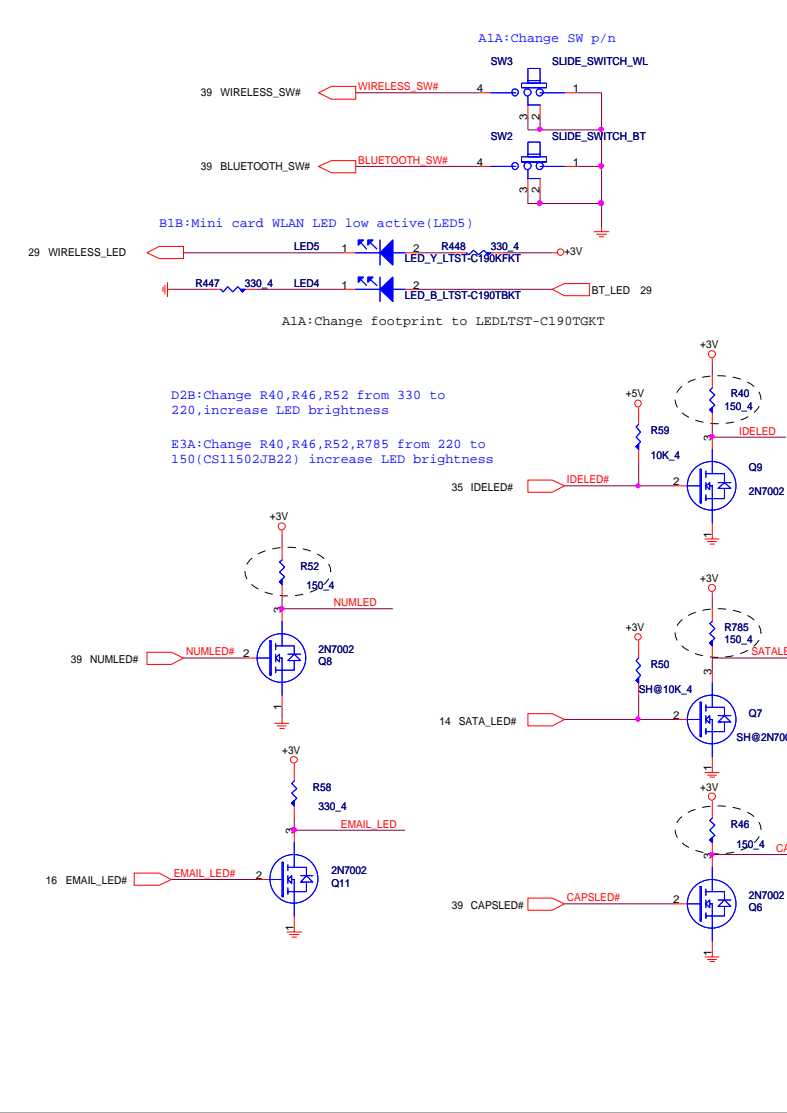
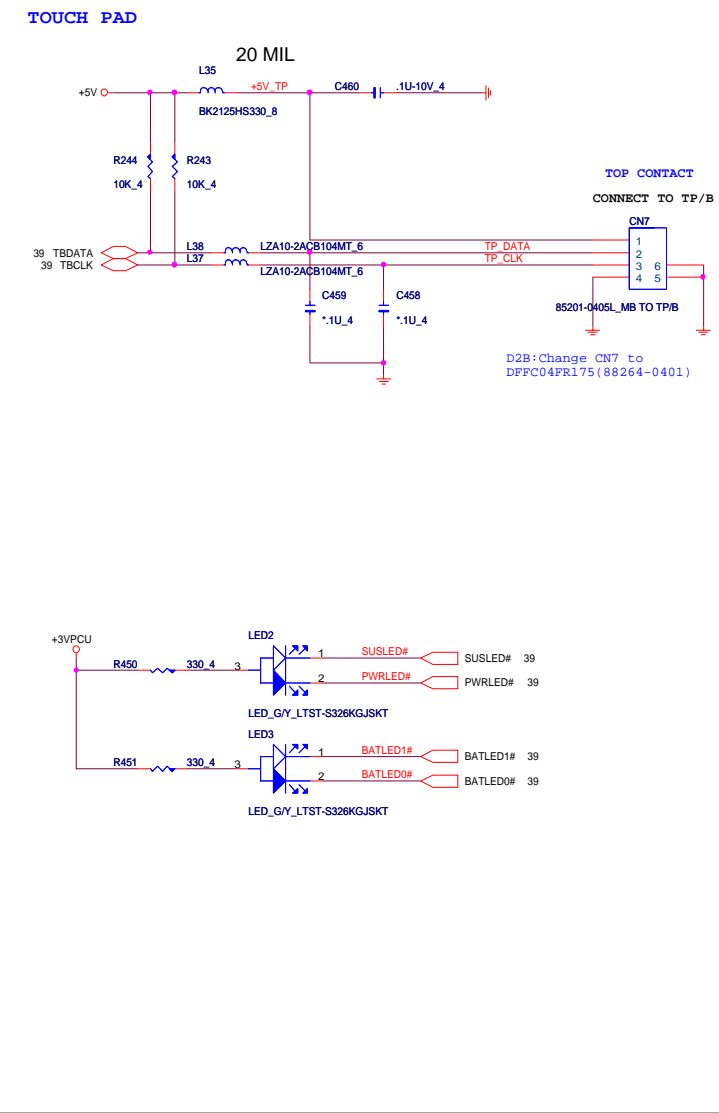
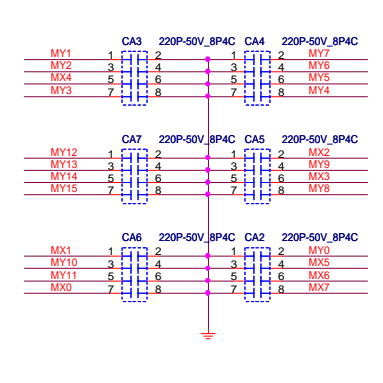
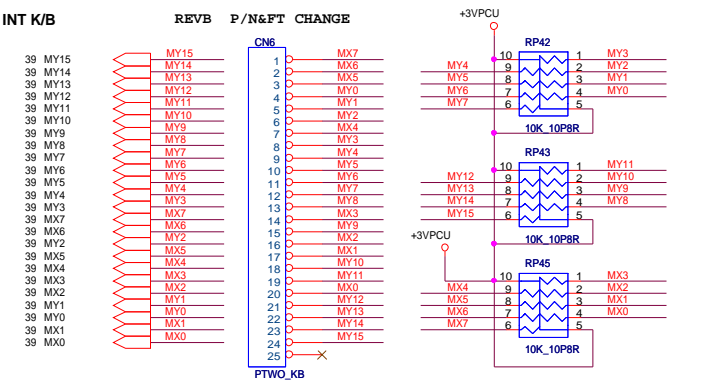
Size	Document Number	Rev
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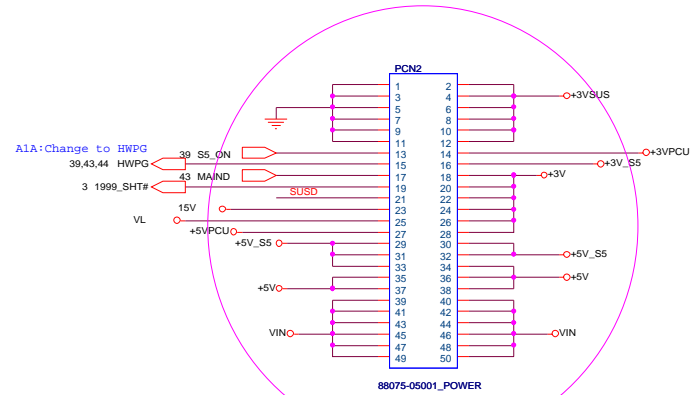






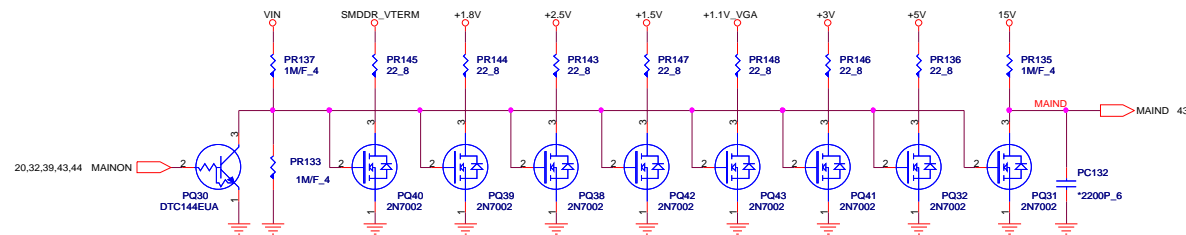
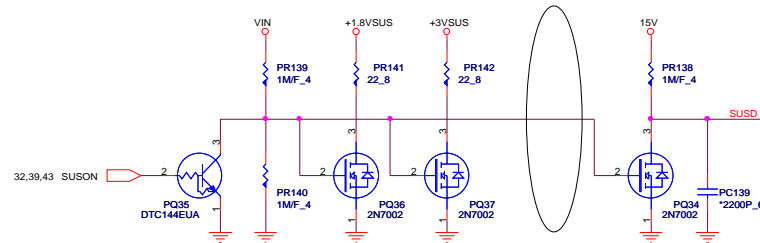






8/2 UPDATE CONN PIN DEFINE

A1A:Del +5VSUS discharge



PROJECT : ZC1  
Quanta Computer Inc.

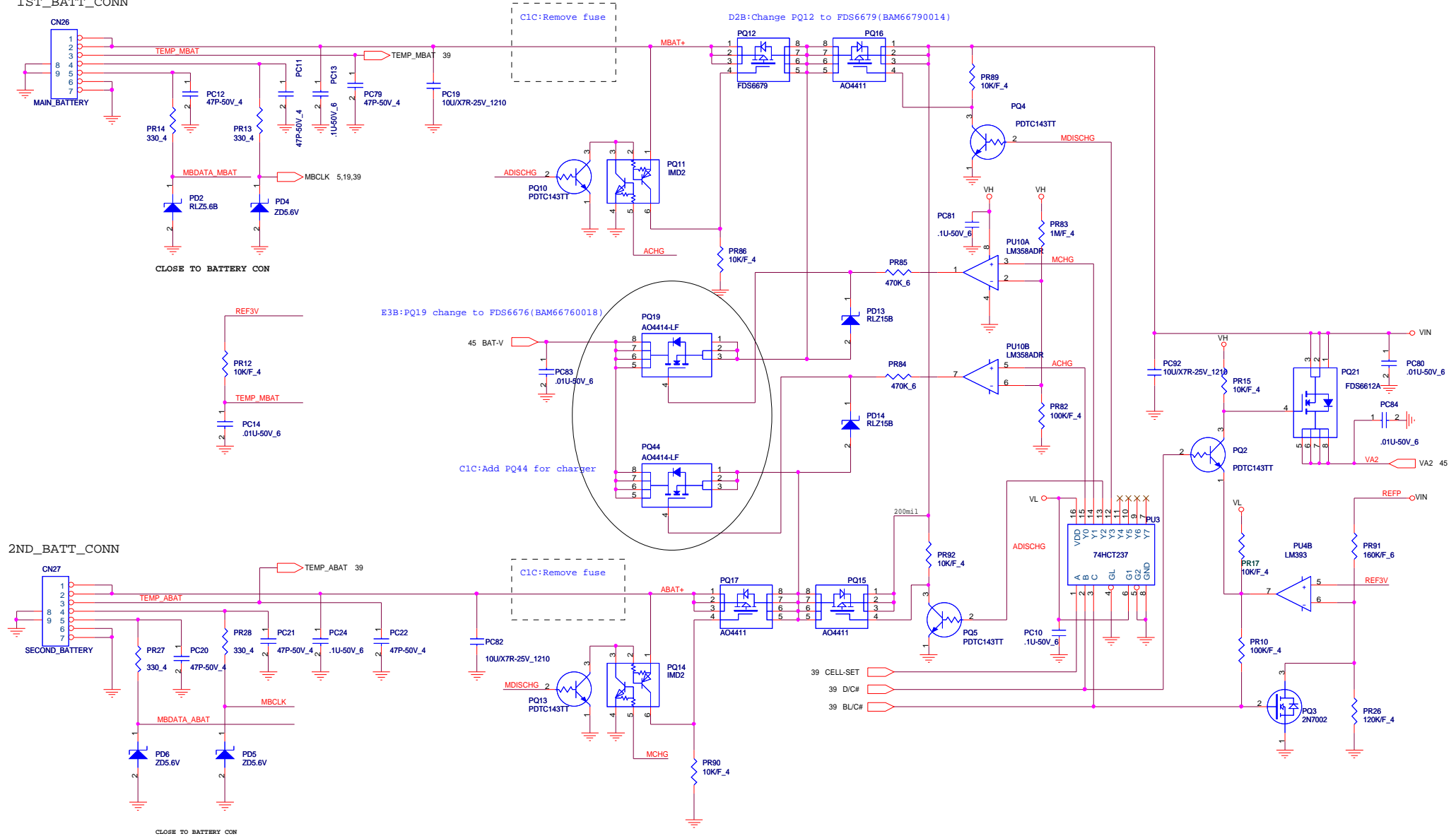




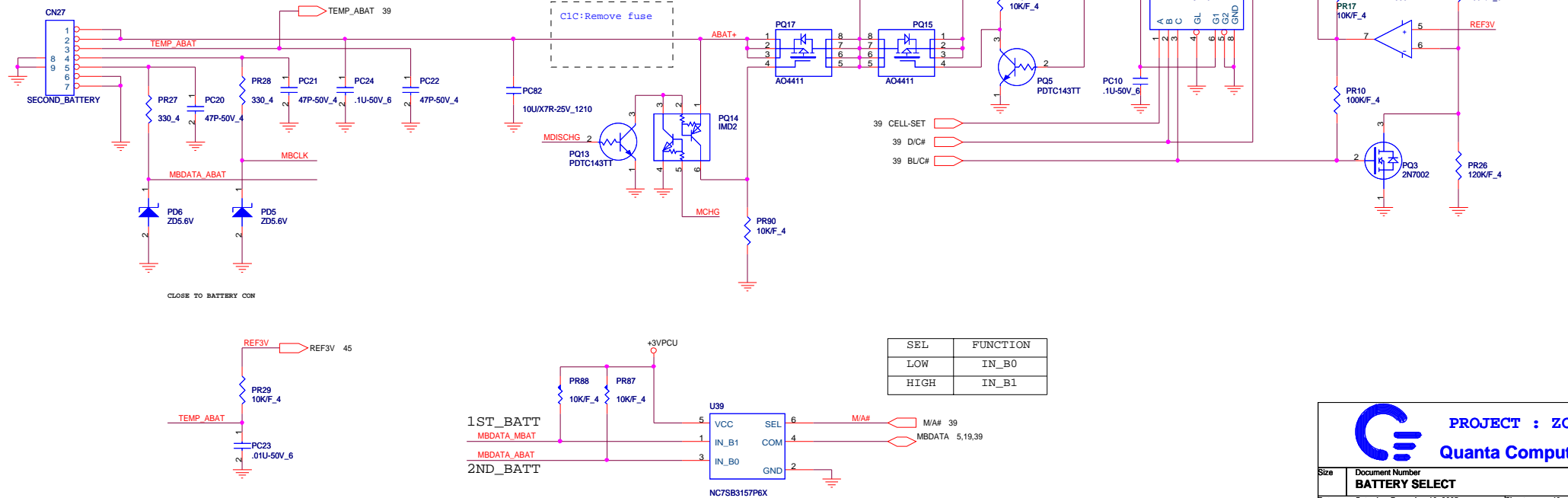


A1A:Change p/n to DFHD07MR391  
B1B:Change CN26 footprint to 20175A-07G1-7P-R

## 1ST\_BATT\_CONN



## 2ND\_BATT\_CONN



SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1